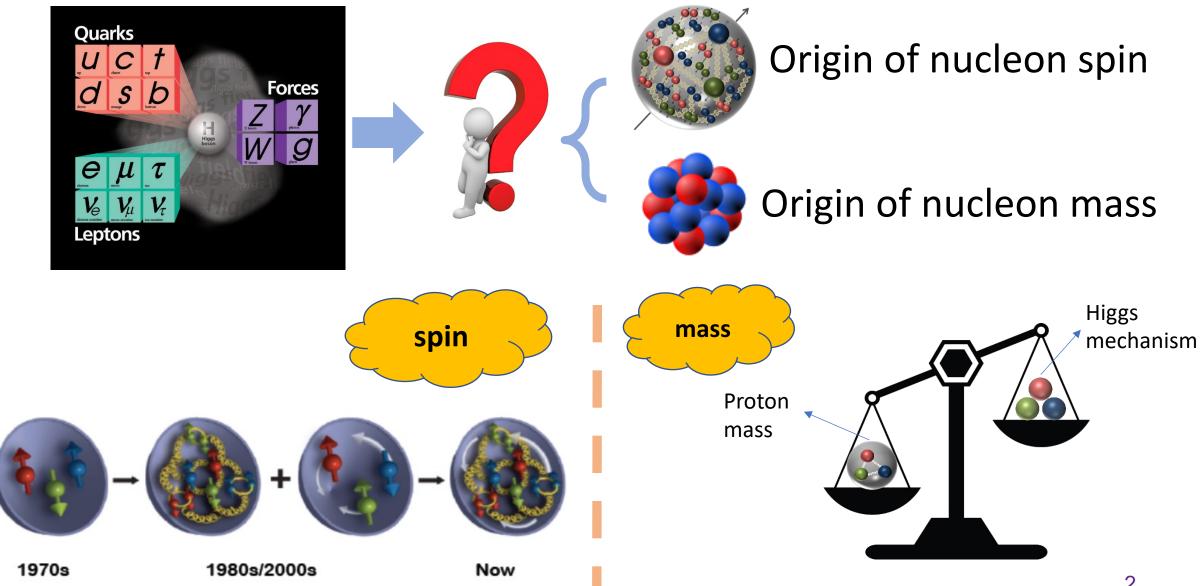


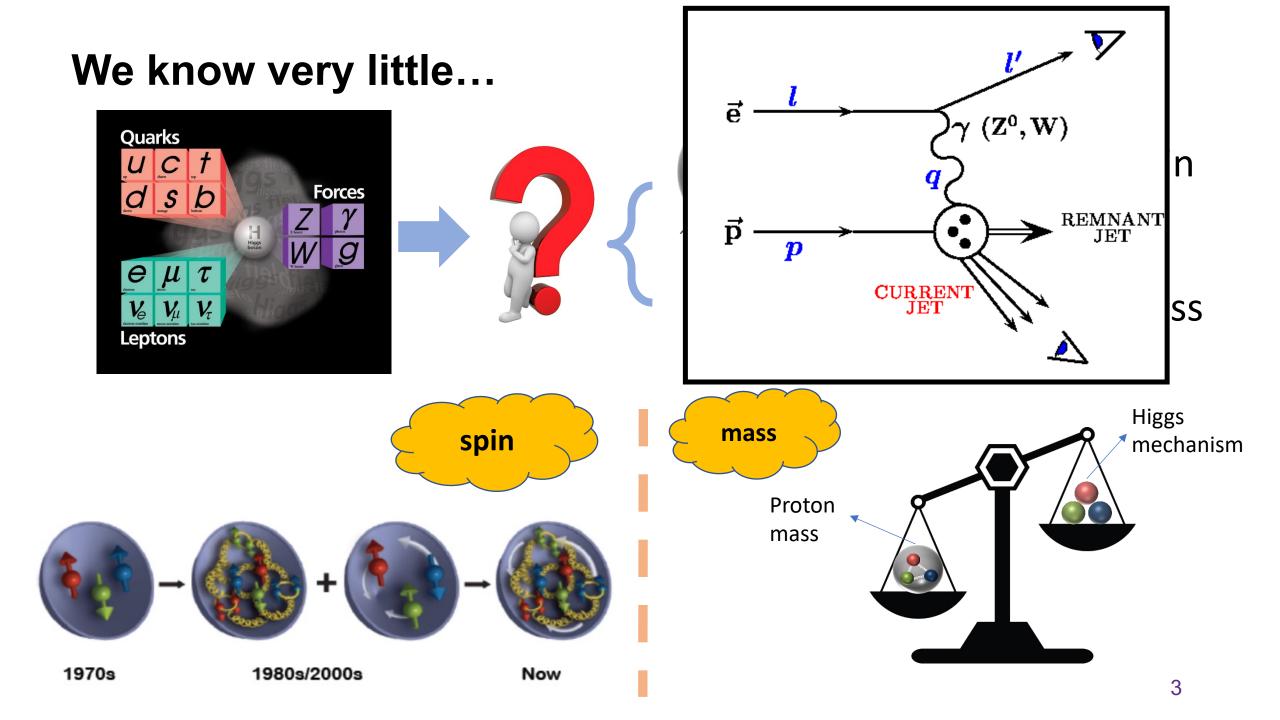
Vertex & tracking detector For EicC

报告人: 郭爱强¹ 赵承心¹ 王亚平² 1 中科院近物所-夸克物质中心 2 华中师范大学-物理科学与技术学院

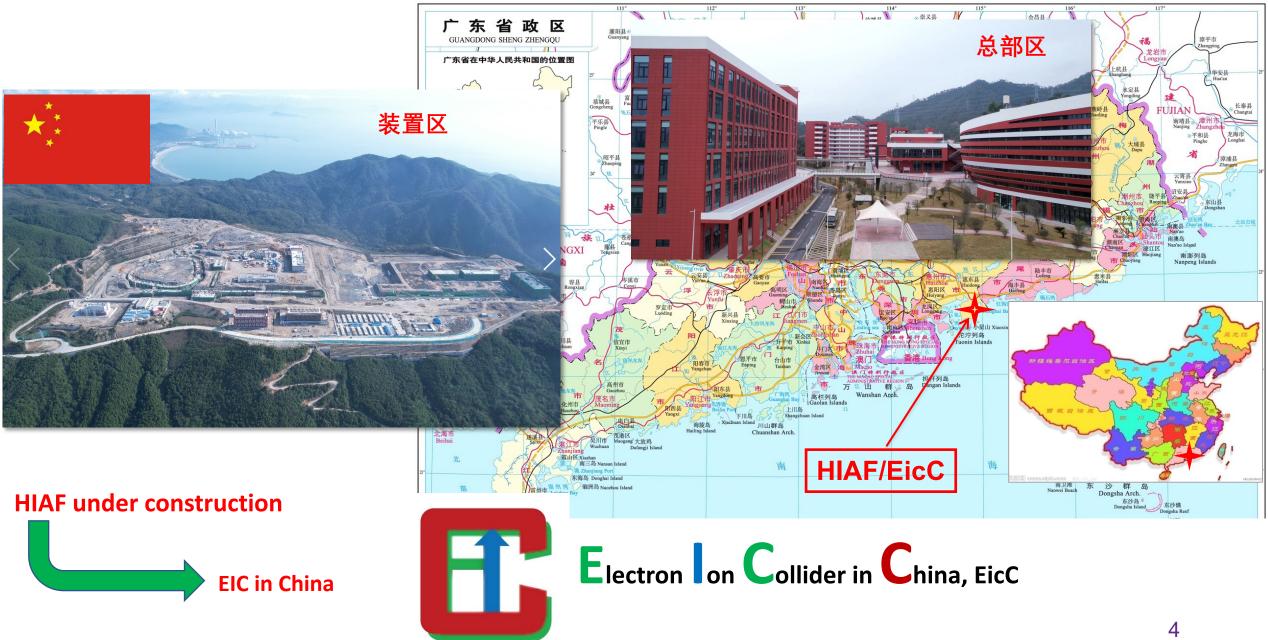
第三届半导体辐射探测器研讨会-2023-05

We know very little...

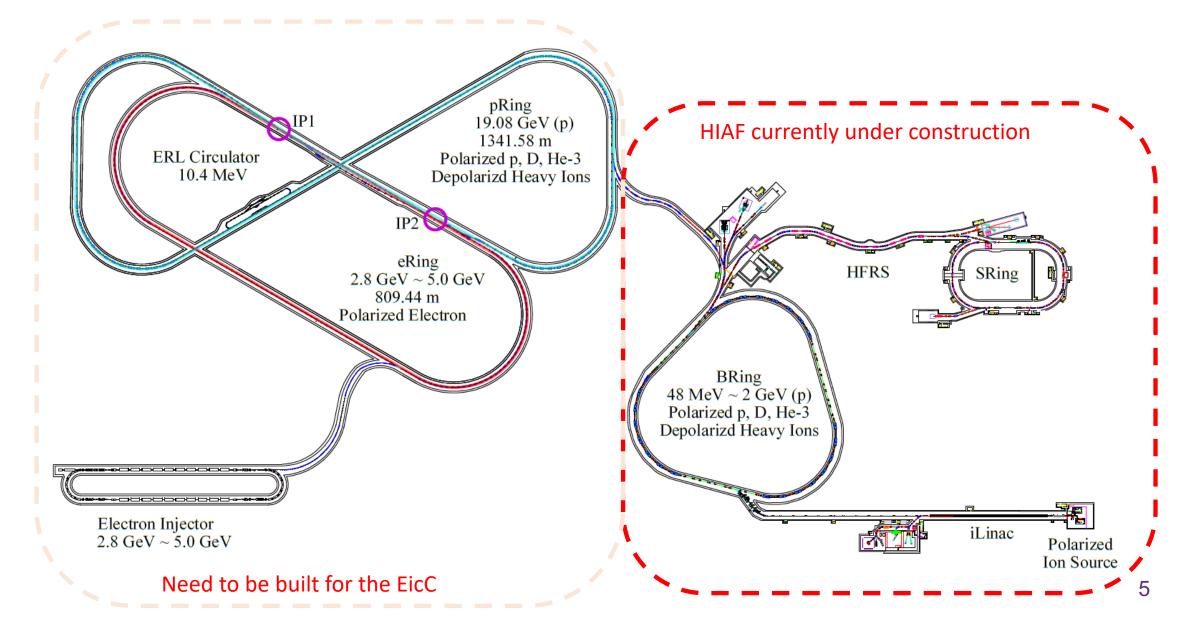




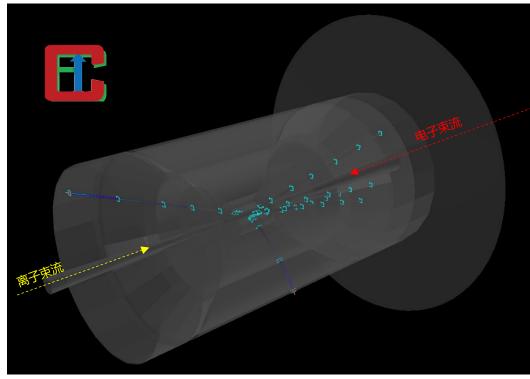
Electron Ion Collider in China...Huizhou(惠州) in Guangdong province

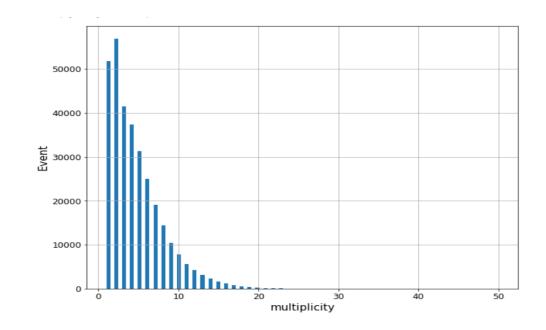


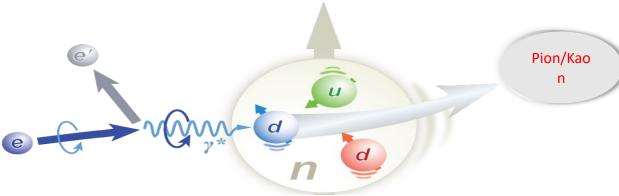
EicC Accelerator complex layout



Data sample @ EicC







- 3.5x20 GeV e-p collision with center of mass energy of 16.7 GeV
- A cross-section of 20.8 µb.
- The luminosity is $L = 2 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}$
- Expect to collect 50 fb⁻¹ per year

The requirement on EicC

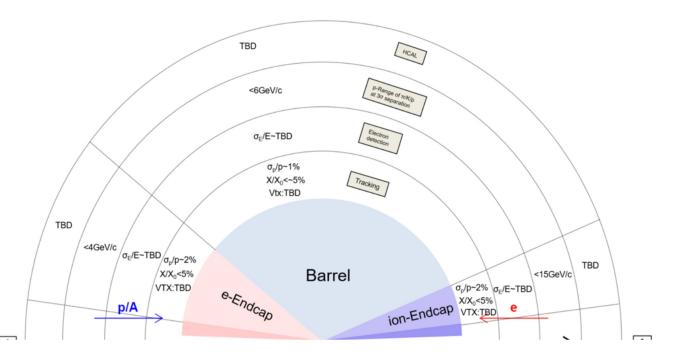
Goal of vertex and tracking system

- Reconstruct charged-particle trajectories
 - Join hits to form a track
 - measure momentum and charge (with magnetic field)
- Reconstruct vertices
 - "primary" vertex: collision point where most particle are produced
 - "secondary" vertices: decay of unstable particles

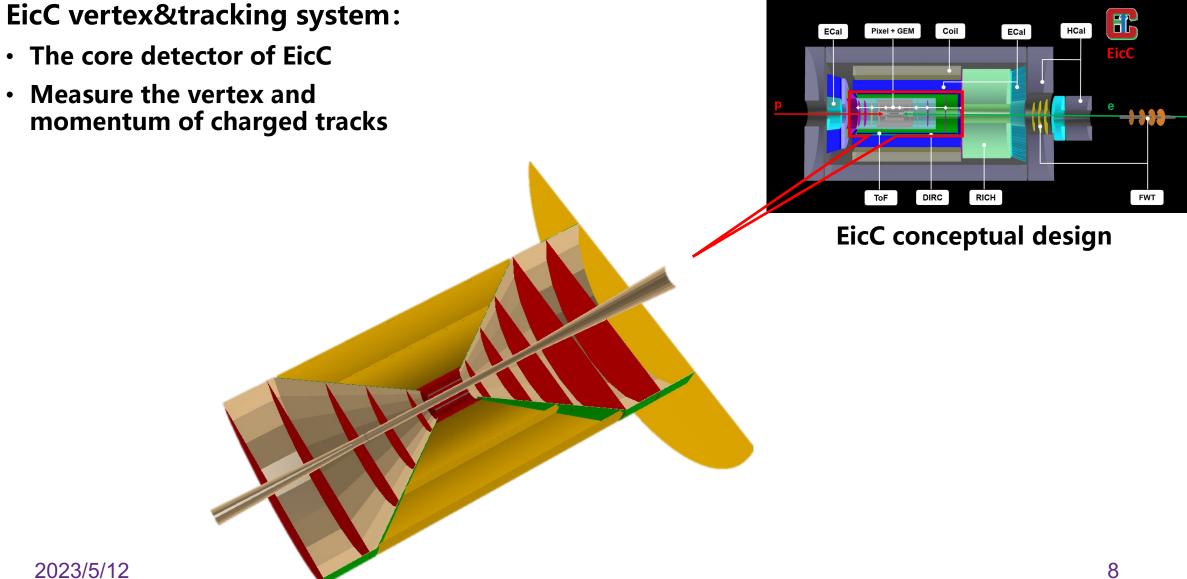
Physics requirements for EicC \rightarrow

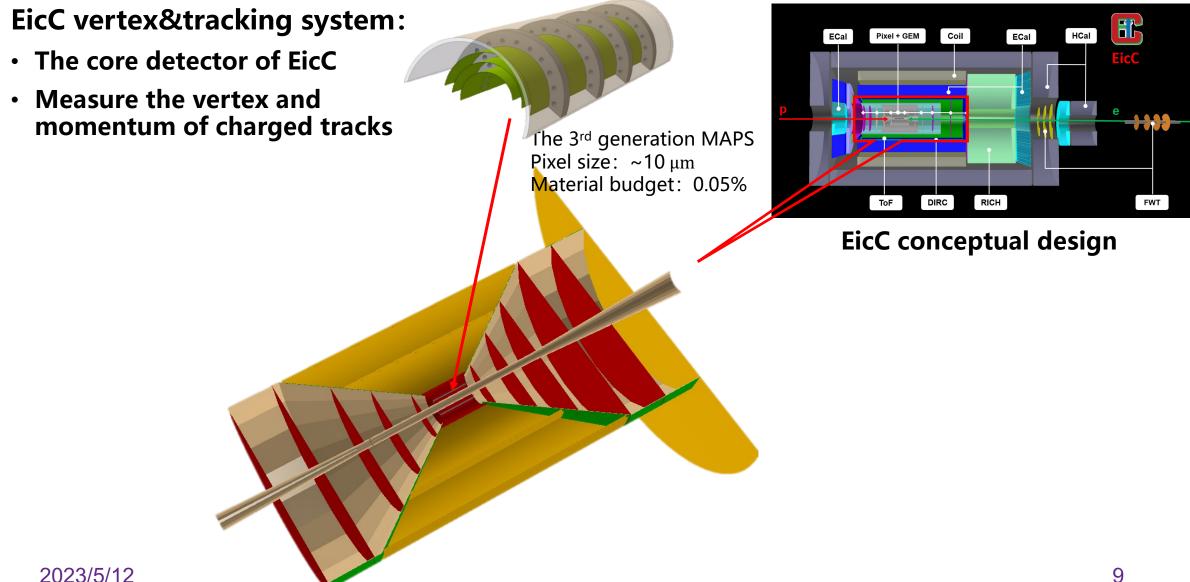
- Barrel ($-1 < \eta < 1.6$):
 - $\frac{\sigma_p}{p} < 1\% @ 1 GeV; \frac{X}{X_0} < 5\%;$
- e-endcap $(-3 < \eta < -1)$:
 - $\frac{\sigma_p}{p} < 2\% @ 1 GeV; \frac{X}{X_0} < 5\%;$
- lon-endcap (1.6 < η < 3):
 - $\frac{\sigma_p}{p} < 2\% @ 1 GeV; \frac{X}{X_0} < 5\%;$
- Assume B ~ 1.5 T

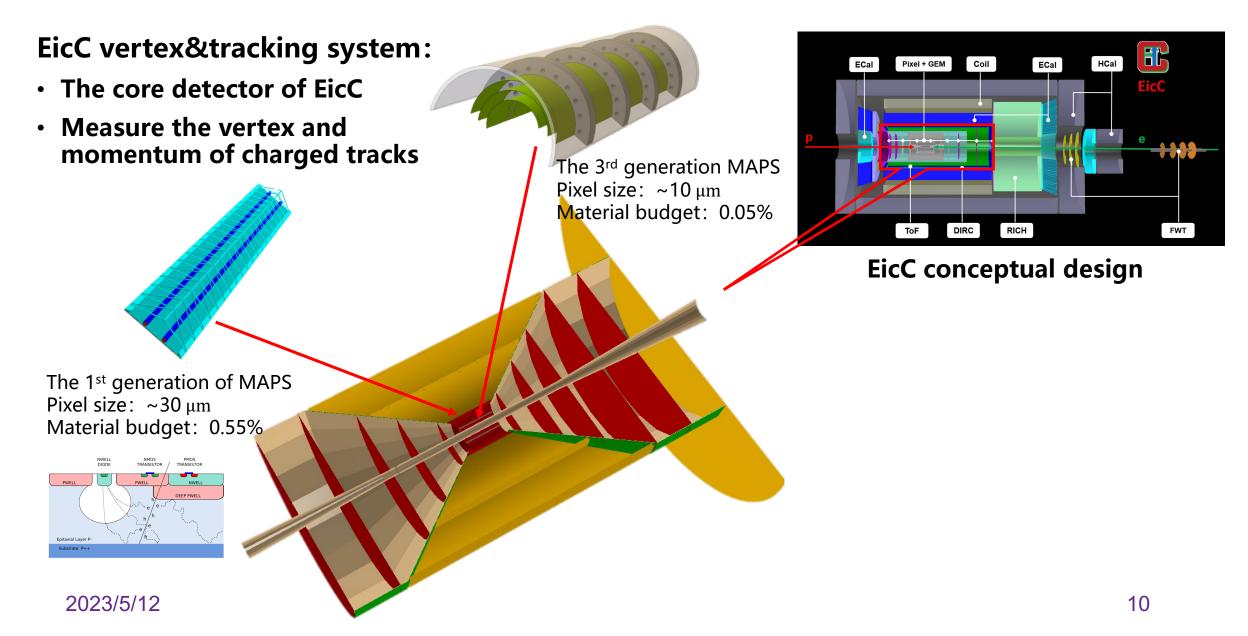
Front. Phys. 16(6), 64701 (2021)

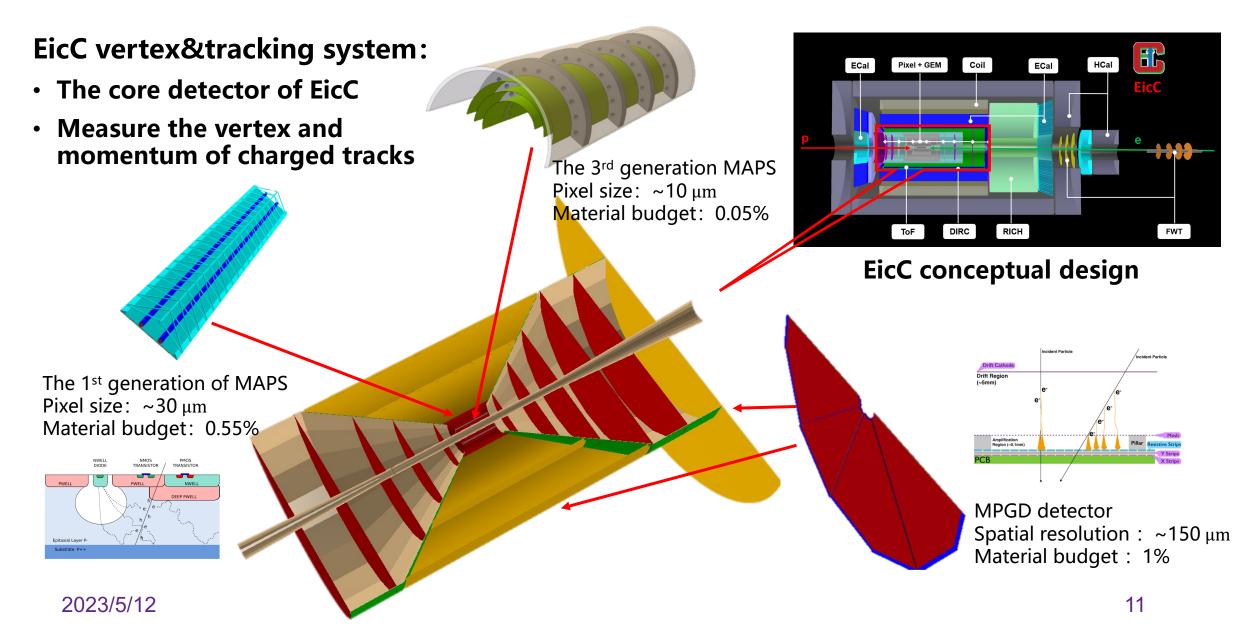


- The event rate of 83.2 kHz.
- the final state particles are concentrated near pseudo-rapidity η = 1, with a particle density rate of dN/dηdt = 8 × 10⁴/s.



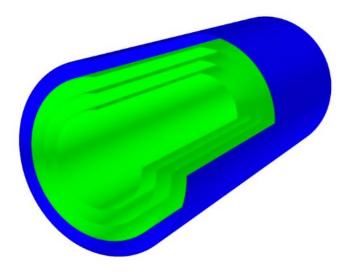




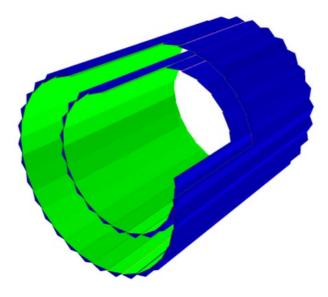


The silicon components

3 ITS3 Layers + Support Layer



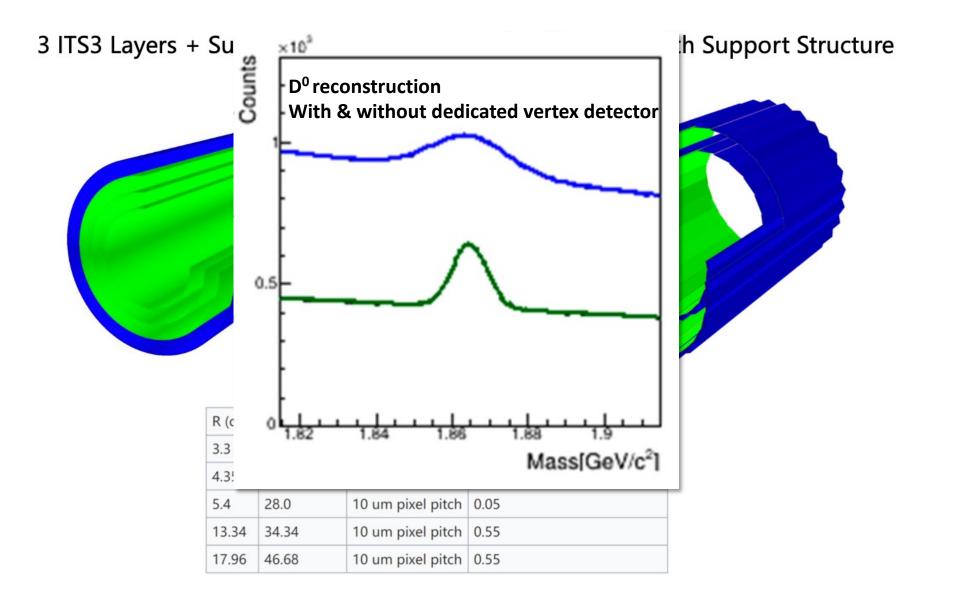
2 ITS2 Layers with Support Structure



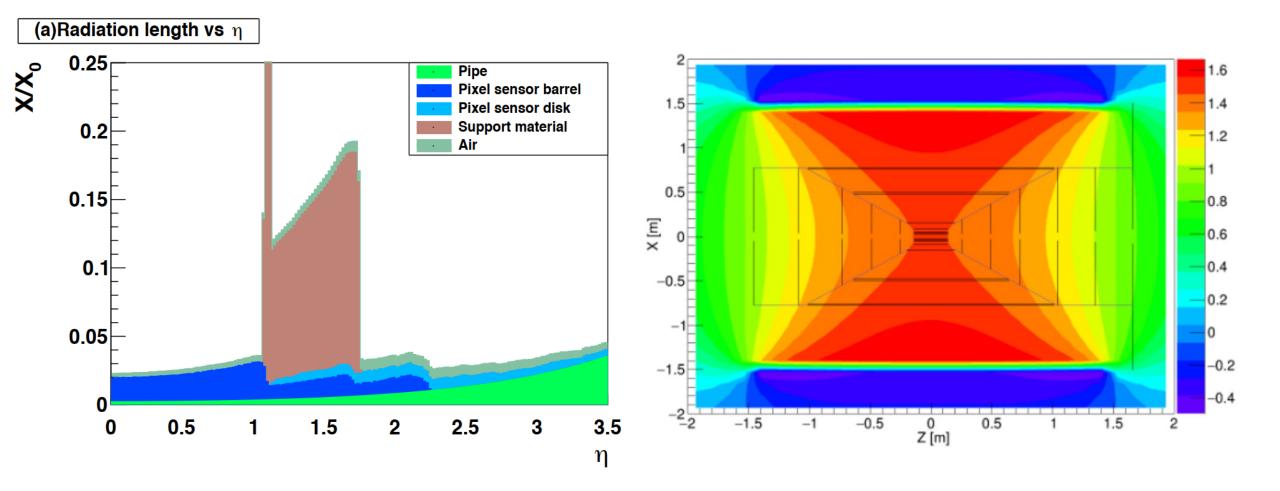
Silicon Tracker (3 Vertex + 2 Barrel Layers)

R (cm)	Length (cm)	Resolution	Active Area Material (X/X0 %)
3.3	28.0	10 um pixel pitch	0.05
4.35	28.0	10 um pixel pitch	0.05
5.4	28.0	10 um pixel pitch	0.05
13.34	34.34	10 um pixel pitch	0.55
17.96	46.68	10 um pixel pitch	0.55

The silicon components

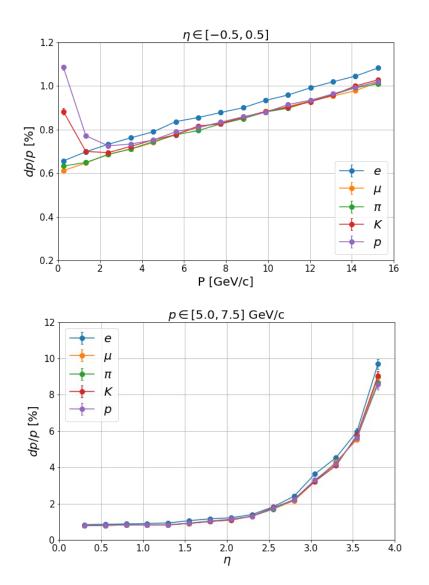


Material budget vs η and B field



14

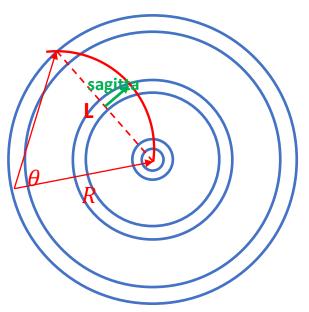
The momentum resolution



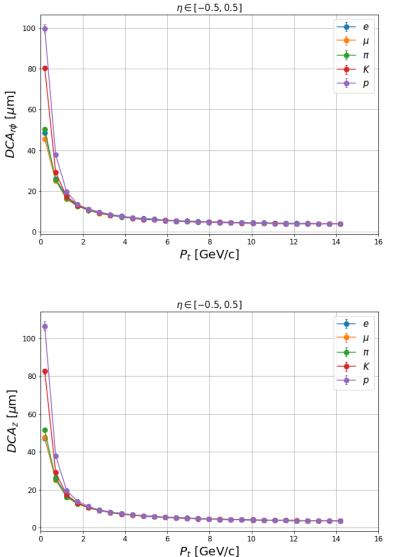
The momentum of a charged track is determined by its trajectory (curvature)

- The formula: p = 0.3 RB, R is the radius of the track, B is the intensity of the magnetic field
- Practically, we measure the sagitta to determine the R:
- The relative momentum resolution is:

$$\frac{\sigma_p}{p} = \frac{\sigma_s}{s} = \frac{8p}{0.3BL^2}\,\boldsymbol{\sigma}_s$$



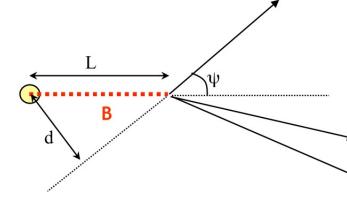
The vertex resolution

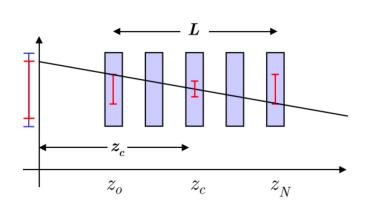


The impact parameter d :

- $d = Lsin\psi$
- ψ is due to multiple-scattering and detector resolution
- In the case of equal spacing detector and equal errors σ
- The uncertainty of measurement on vertex (details in backup):

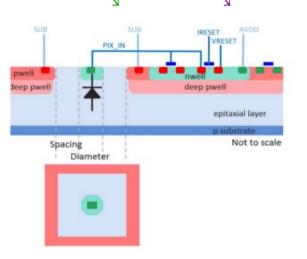
$$\sigma_{vertex}^{2} = \frac{\sigma^{2}}{N+1} + \frac{\sigma^{2}}{N+1} \frac{12N}{N+2} \frac{Z_{c}^{2}}{L^{2}}$$





The Monolithic Active Pixel Sensor

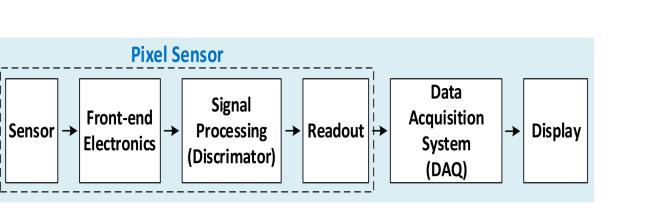
• CMOS Pixel Sensors \equiv Detector \oplus Front-End Electronics in same die

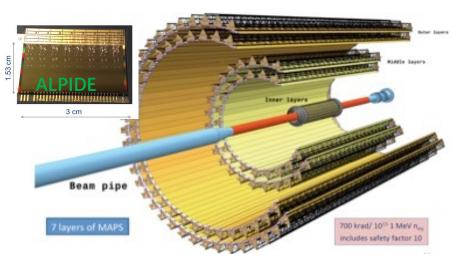


Readout (zero suppression)	PIXEI Array	adout (zero suppression)	Readout (zero suppression)
Bias	、Reado	ut、Co	ntrol



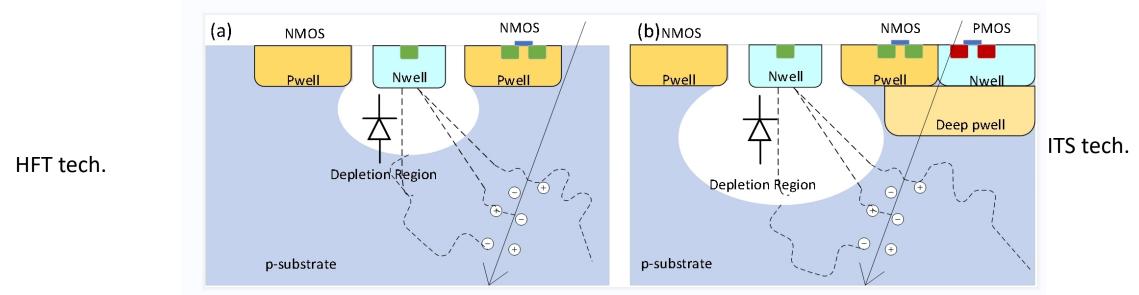
STAR HFT (世界上首个像素探测器) 400片MAPS, 360M pixels



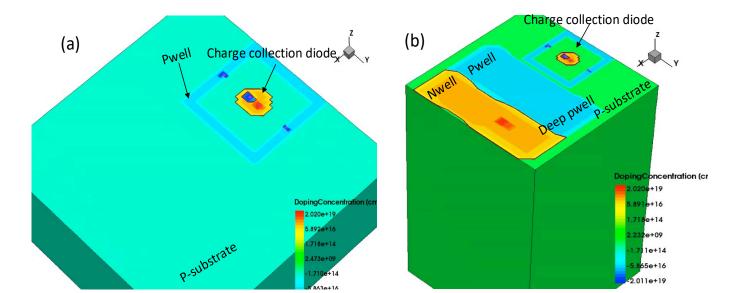


ALICE ITS 探测器 (目前最大规模像素探测器) 24142块MAPS, ~10㎡, 12.5G pixels

TCAD simulation

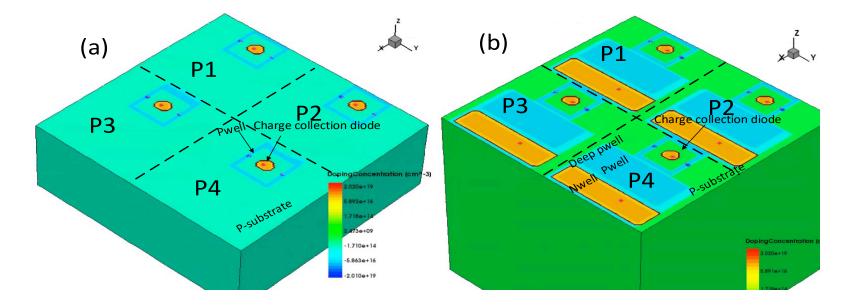


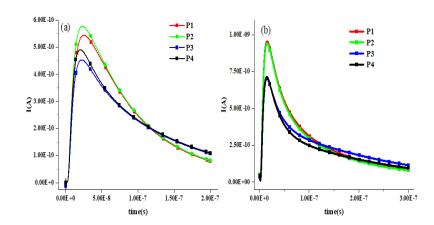
工艺选择和比较:标准双阱工艺 vs 四阱工艺



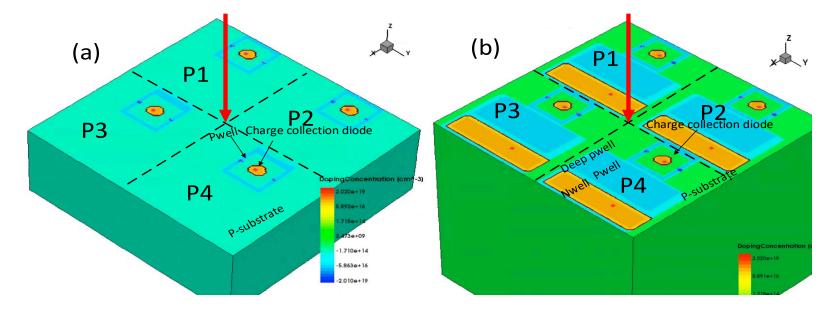
18

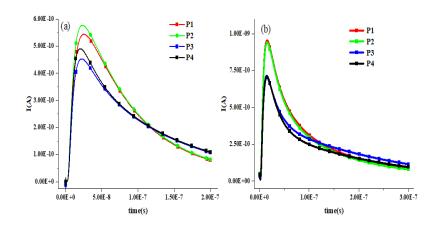
TCAD simulation





TCAD simulation

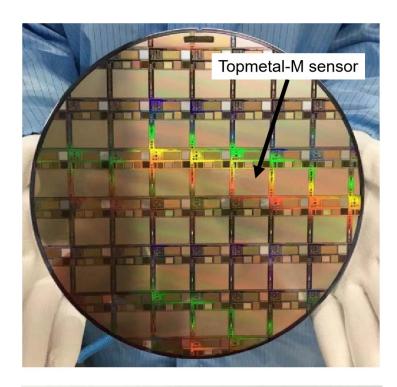


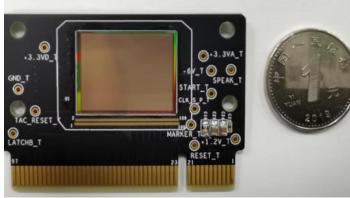


Pix	P1	P 2	P 3	P 4	
Change	Twin-well LR process	329	340	300	308
Charge collection	Quad-well HR process	551	530	499	450

50~60% improvement

The first MAPS based on domestic technology





- Topmetal-M

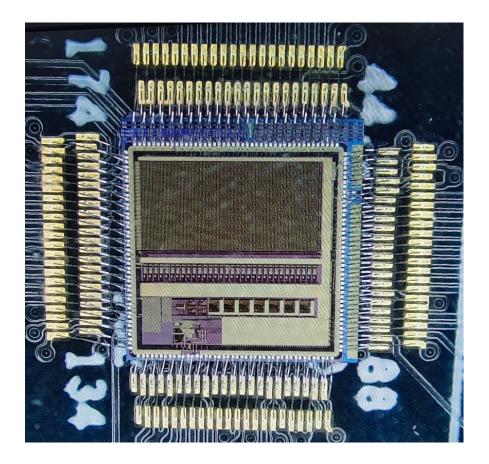
中科院战略先导B"核物质相结构与重元素合成研究"专项支持

- 近物所IMP SLIMP & 华师CCNU PLAC
- 基于国内四阱高阻衬底工艺
- 2018.05 2019.12设计制造
- 2020.01 2021.12测试验证

Parameters:

- 像素阵列 512 x 400 Pixels
- 40umx 40um
- Time, Energy and Position Measurement
- Thinned to 100um from backsid
- 兼具电荷搜集型Topmetal和MAPS

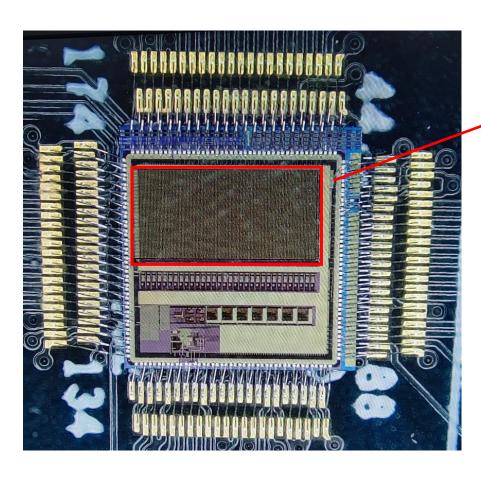
The full functional MAPS based on domestic technology - Nupix-A1

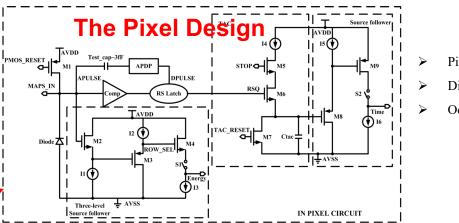


- □中科院战略先导B"核物质相结构与重 元素合成研究"专项支持、EicC原型芯 片
 □近物所像素研究室SLIMP牵头研发
- □位置、时间和能量测量
- □目的:验证基于国内工艺开发复杂度 高的像素芯片

The full functional MAPS based on domestic technology

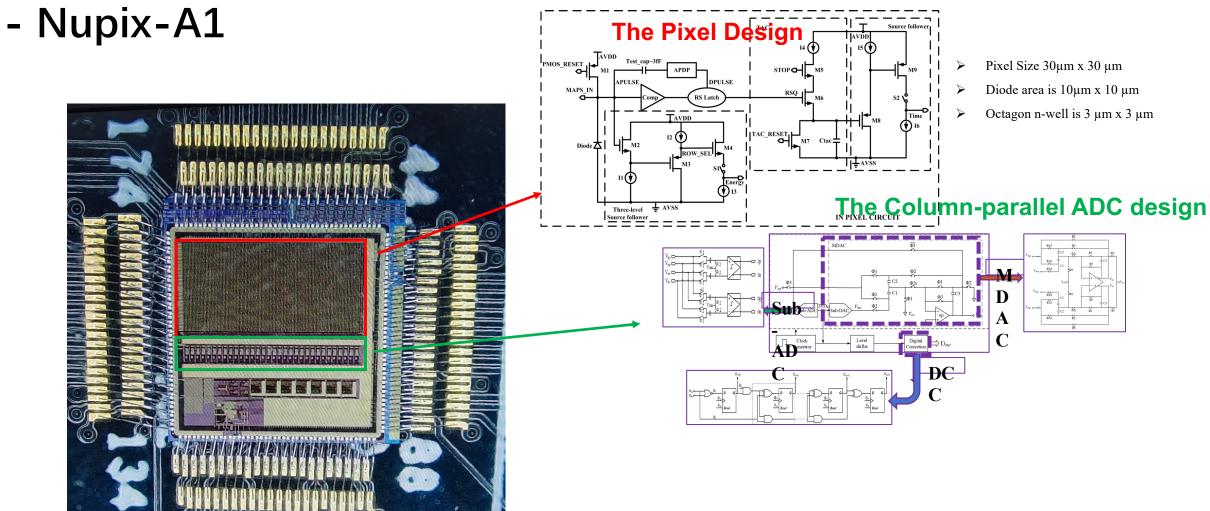
- Nupix-A1



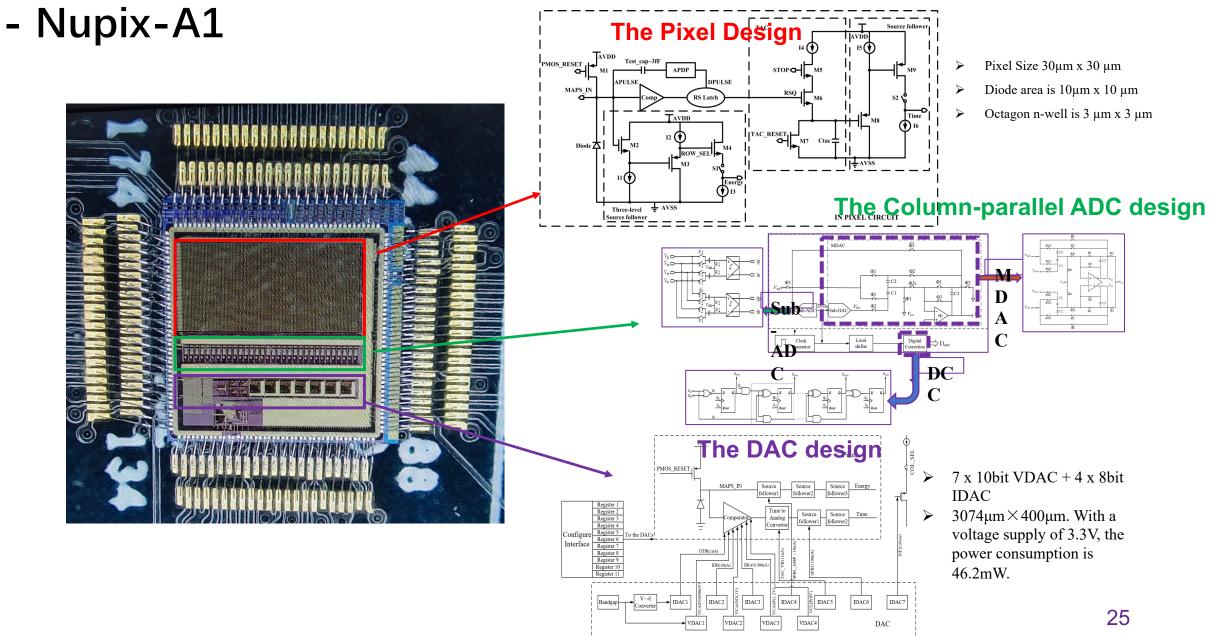


- Pixel Size 30µm x 30 µm
- Diode area is 10µm x 10 µm
- Octagon n-well is 3 µm x 3 µm

The full functional MAPS based on domestic technology



The full functional MAPS based on domestic technology

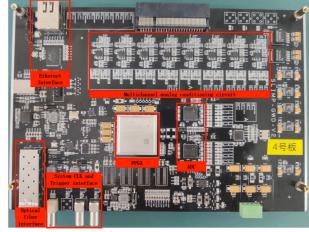


Radiation-hardened front-end electronics

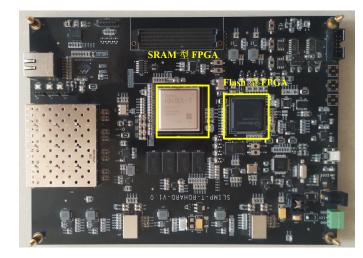
Flash Based



Sram Based

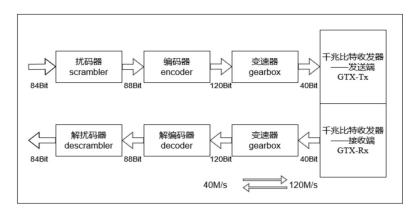


Sram based 三模重刷

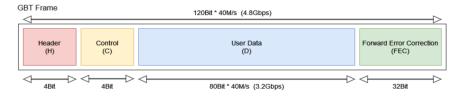




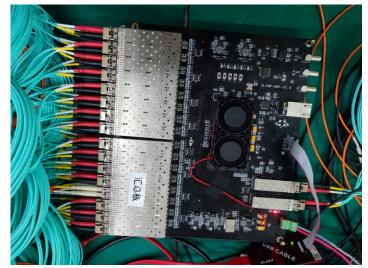




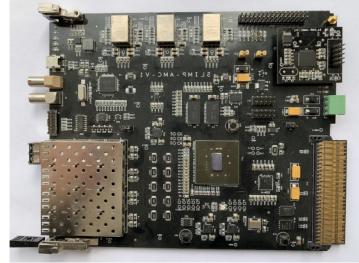
GBT-FPGA



high speed back-end electronics

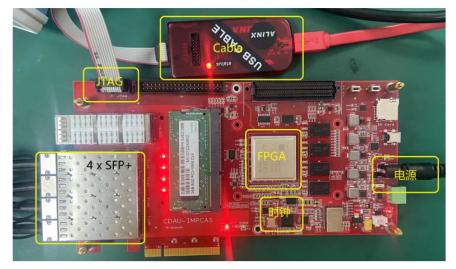


32路光纤汇总,两路万兆以太网数 据汇总板。其中主要FPGA为Vertex-7.



HP-FMC USB3.0 USB3.0 FPGA DDR4 DDR4 Power Power OPCIe Interface

ultra-scale的数据汇总板,其中PCle 提供了大于50gbps的数据通路



MircoTCA的数据汇总板

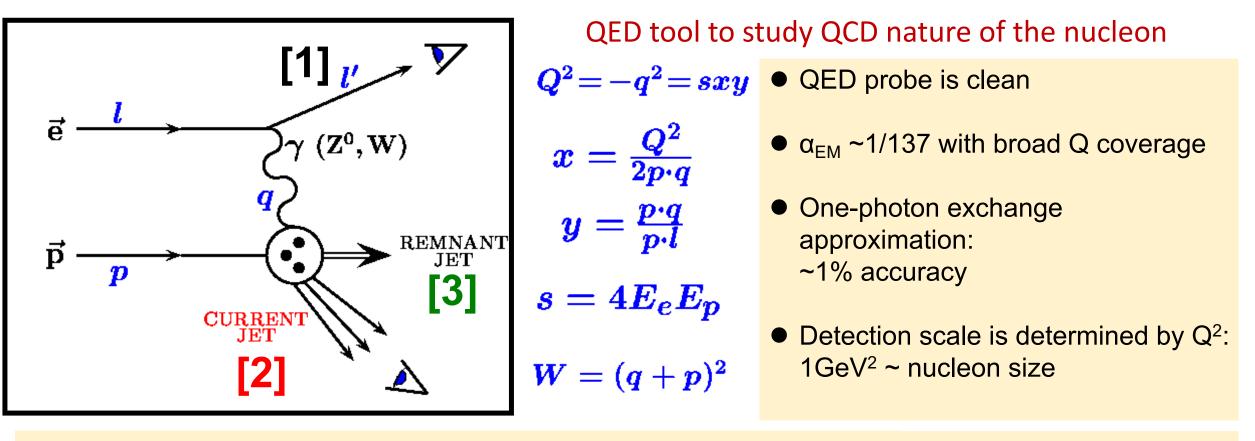
Summary

- Sillicon + MPGD vertexing and tracking detector is designed to fit the requirement of EicC
- The full simulation of the geometry design is done to validate the performance
- The full functional MAPS based on domestic technology Nupix-A1 is developed by IMP SLIMP & CCNU PLAC
- More efforts are needed to improve the R&D

Thanks for your attention!!

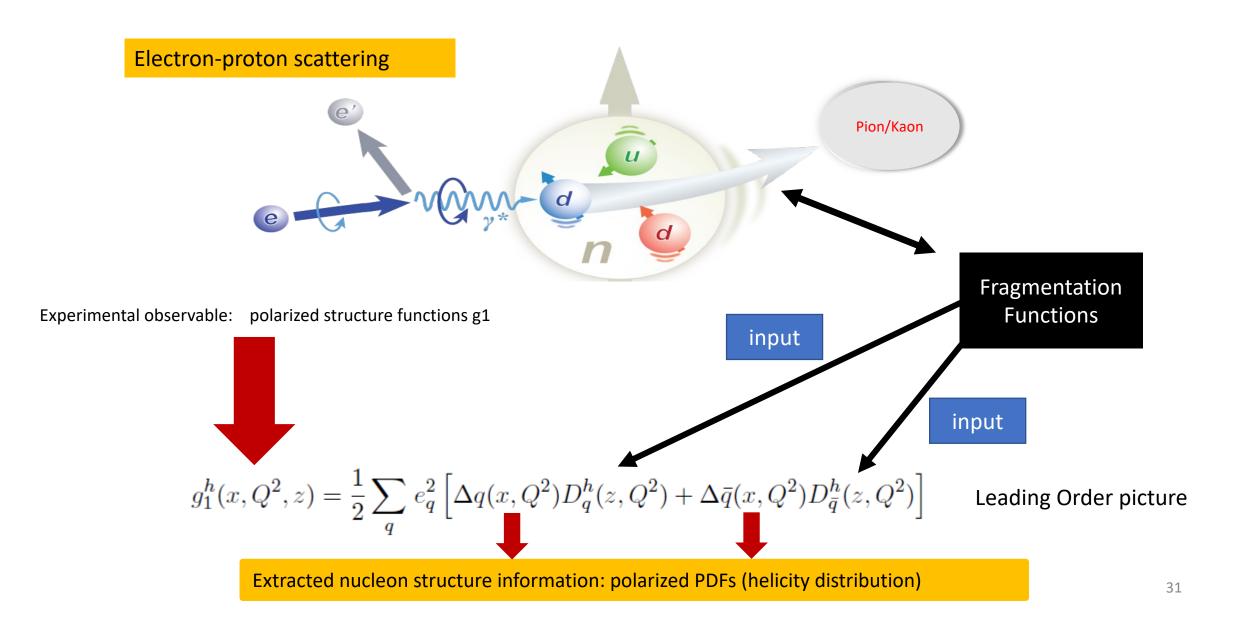
Backup

Lepton-Nucleon Scatterings



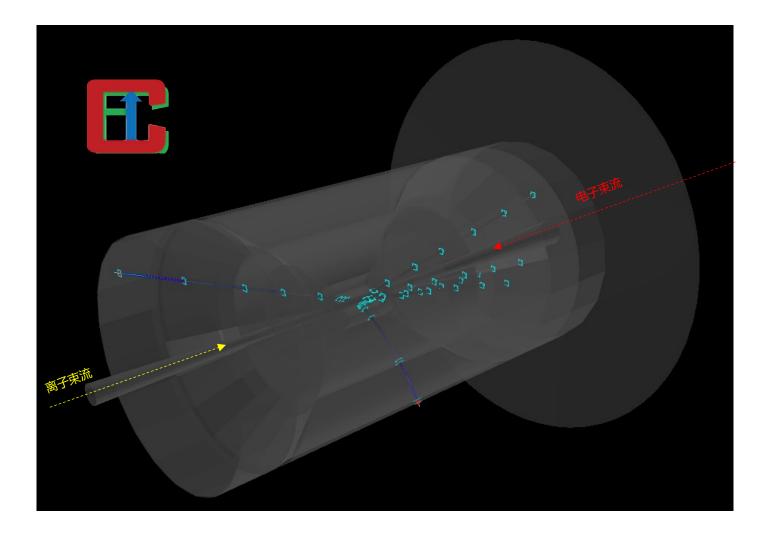
Observe scattered electron/muon Observe current jet/hadron Observe remnant jet/hadron as well [1] → inclusive
 [1]+[2] → semi-inclusive
 [1]+[2]+[3] → exclusive

SIDIS processes for flavor decompositions



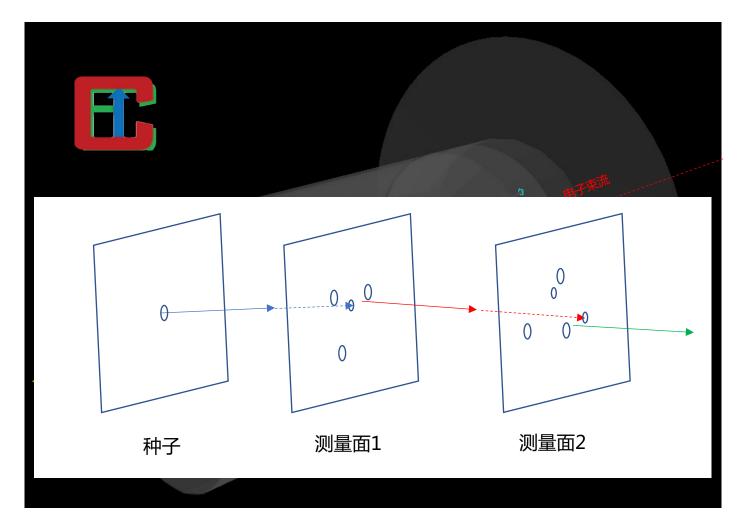
Track reconstruction

- No dedicate track finding algorithm is implemented
- Find track candidate according to the MC information
- Track candidates are fitted by Kalman fitter method



Track reconstruction

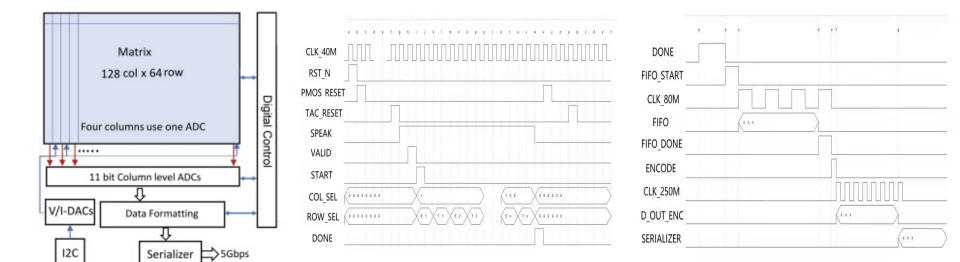
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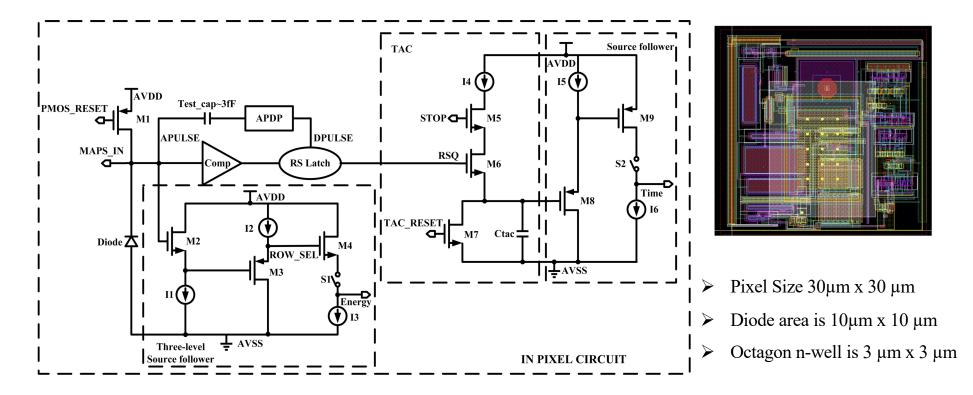
The Digital Control Design

Pixel-to-pixel scan in each region

Chip-level data processing

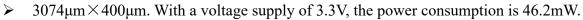


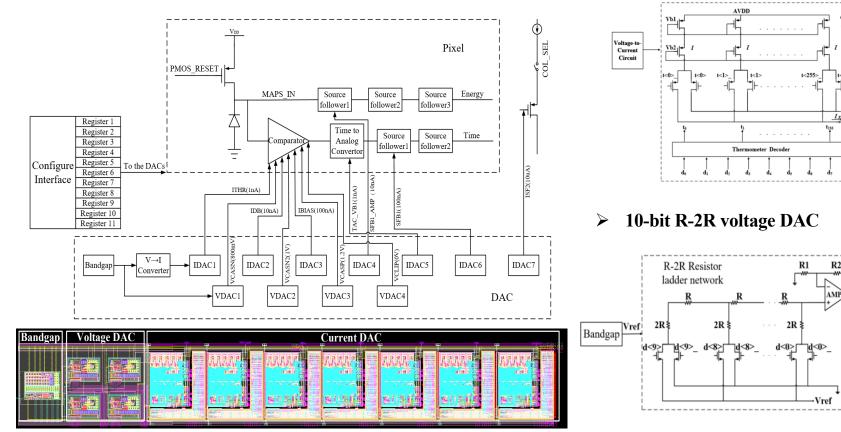
The Pixel Design



The DAC design

7 x 10bit VDAC + 4 x 8bit IDAC \geq





➢ 8-bit current-steering type DAC

Current-

Steering

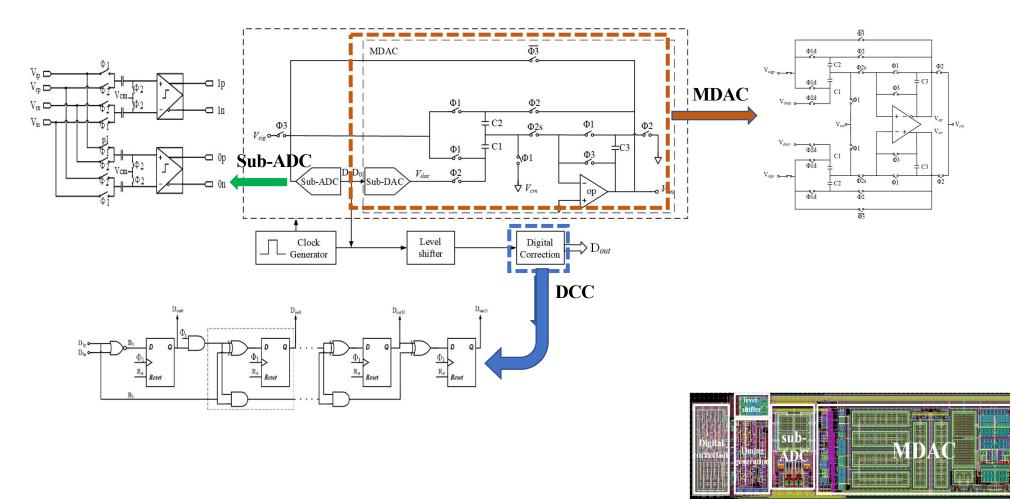
t<255>

 $\xrightarrow{I_{\Sigma}}$ Iout

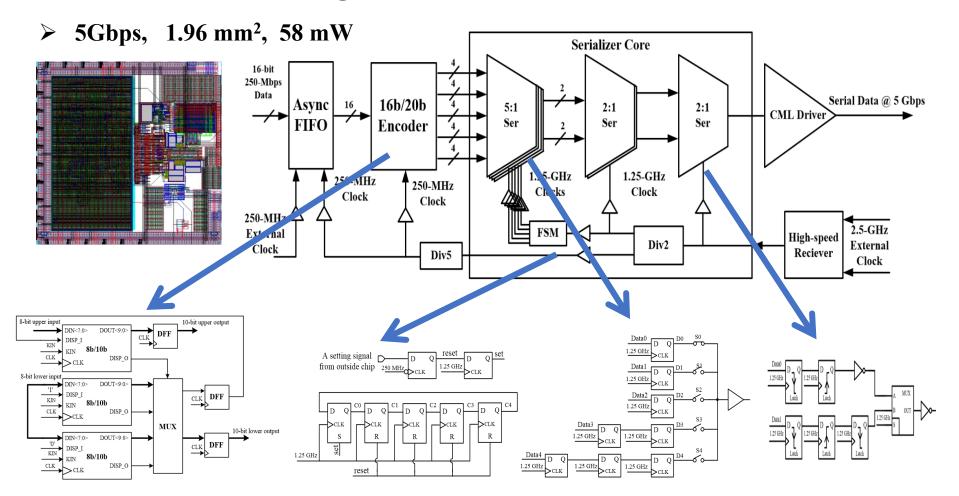
R2

The Column-parallel ADC design

- Dsigned in a fully differential cyclic architecture and takes 11 clock cycles to to generate 12bit output
- ➤ 3.63Msps x 12bit, 380×100 μm², 7.6mW@3.3V

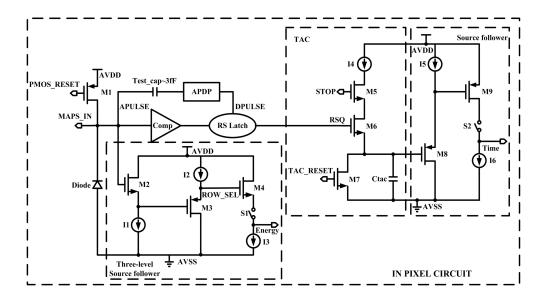


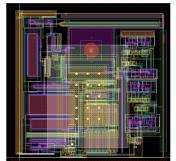
The Serializer Design



The Pixel and DAC design

The Pixel Design





- Pixel Size 30μm x 30 μm
- > Diode area is $10\mu m \ge 10 \mu m$
- > Octagon n-well is $3 \mu m \times 3 \mu m$

The DAC design

- > $7 \times 10bit VDAC + 4 \times 8bit IDAC$
- > $3074\mu m \times 400\mu m$. With a voltage supply of 3.3V, the power consumption is 46.2mW.

