中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

SOI像素探测器的研究进展

核探测与核电子学国家重点实验室&核物理与核技术国家重点实验室
2019年联合年会

卢云鹏

2019-4-22

报告内容

- SOI像素探测器的概念
  - SOI集成电路工艺
  - SOI像素探测器工艺
- Motivation
- 关键技术问题
- R&D Activities
  - SOFIST系列芯片（for ILC）
  - CPV系列芯片（for CEPC）
- SOI技术展望

SOI集成电路工艺

- 早期用于处理器
- 现阶段主要用于消费电子
  - 3D camera, 电波手表
  - 2017年市场规模5.4亿美元
- 以及政府出资的研究项目
- Device layer ~50nm
  - 低功耗
  - Latch-up免疫，
    Single Event Effect不敏感

Ref.: SOI-CMOS Device Technology, Yasuhiro FUKUDA etc

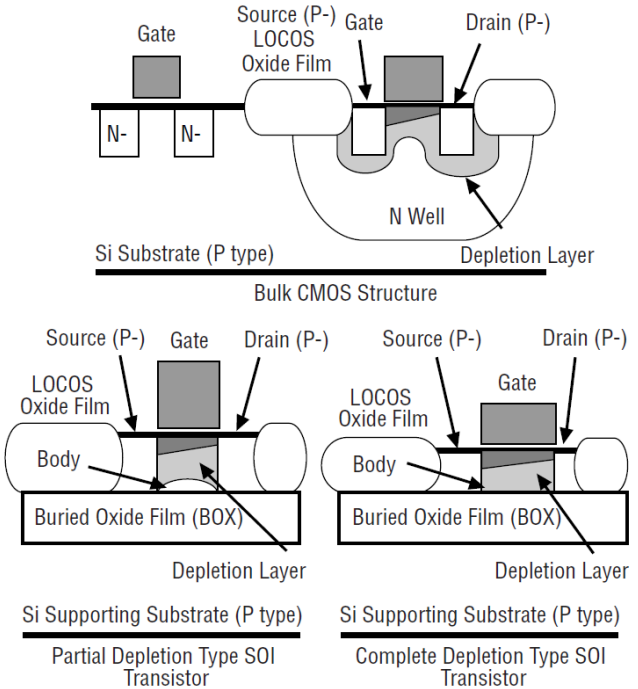


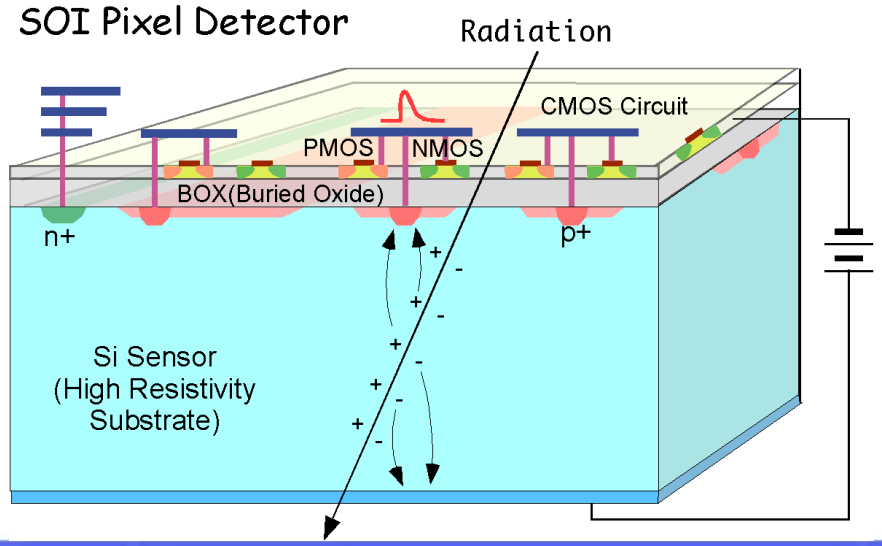
Figure 1: Comparison Between Bulk CMOS and SOI-CMOS Structures

	Bulk CMOS	SOI CMOS Transistor	
	Transistor	Partial Depletion Type	Complete Depletion Type
S Value (mV/dec)	80 to 90	80 to 90	60 to 70
Junction Capacitance (Relative Value)	1	0.1 to 1	0.1
Parasitic Thyrister Structure	Yes	No	No

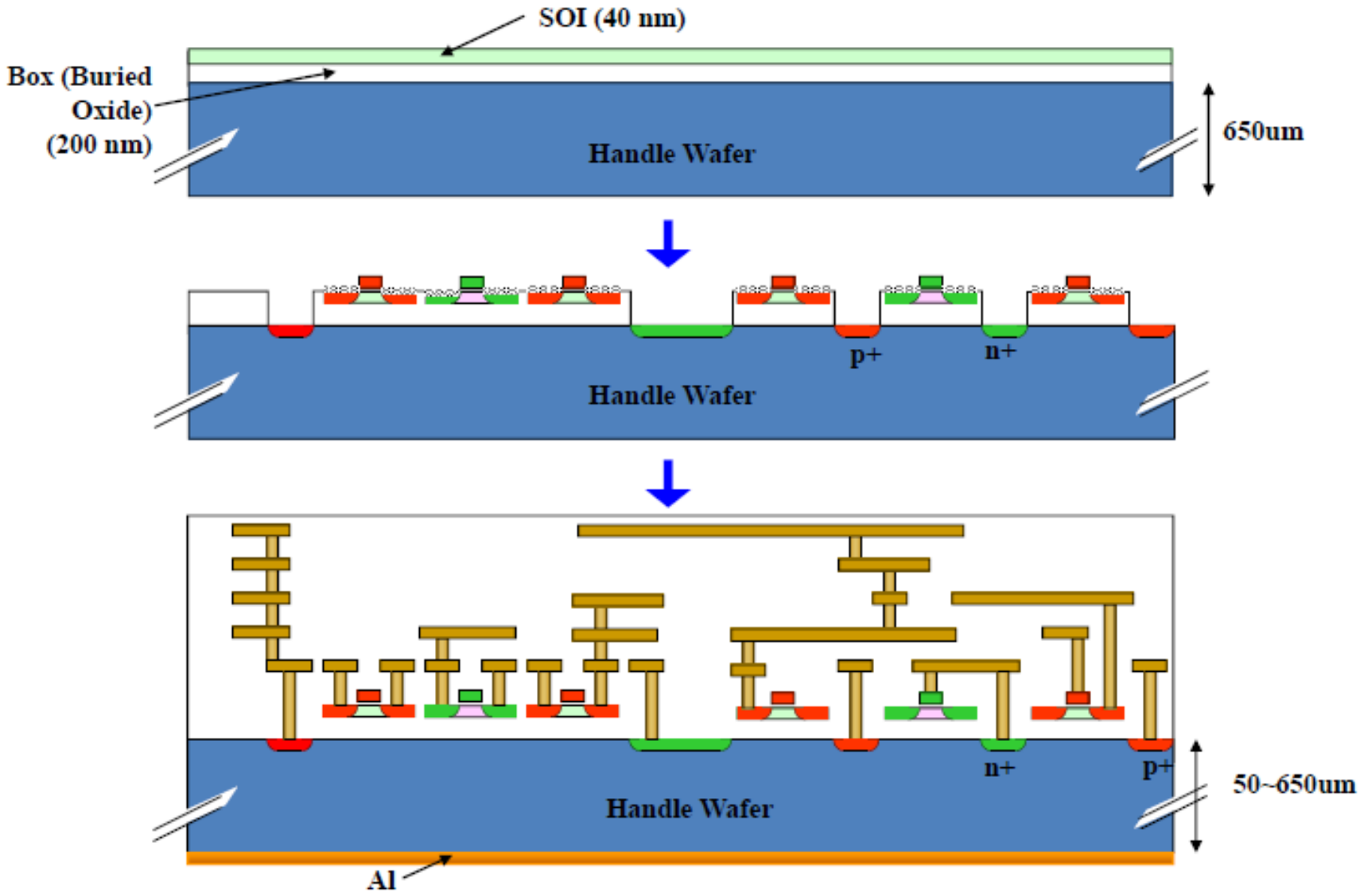
Table 1: Transistor Performance Comparison

SOI像素探测器工艺

- 三明治结构
  - 上：以像素为单元的独立信号处理电路（Device Layer），继承了SOI集成电路的优点
  - 中：SiO_2绝缘层（金属通孔阵列实现一对一电连接）
  - 下：以像素为单元的sensor diode阵列

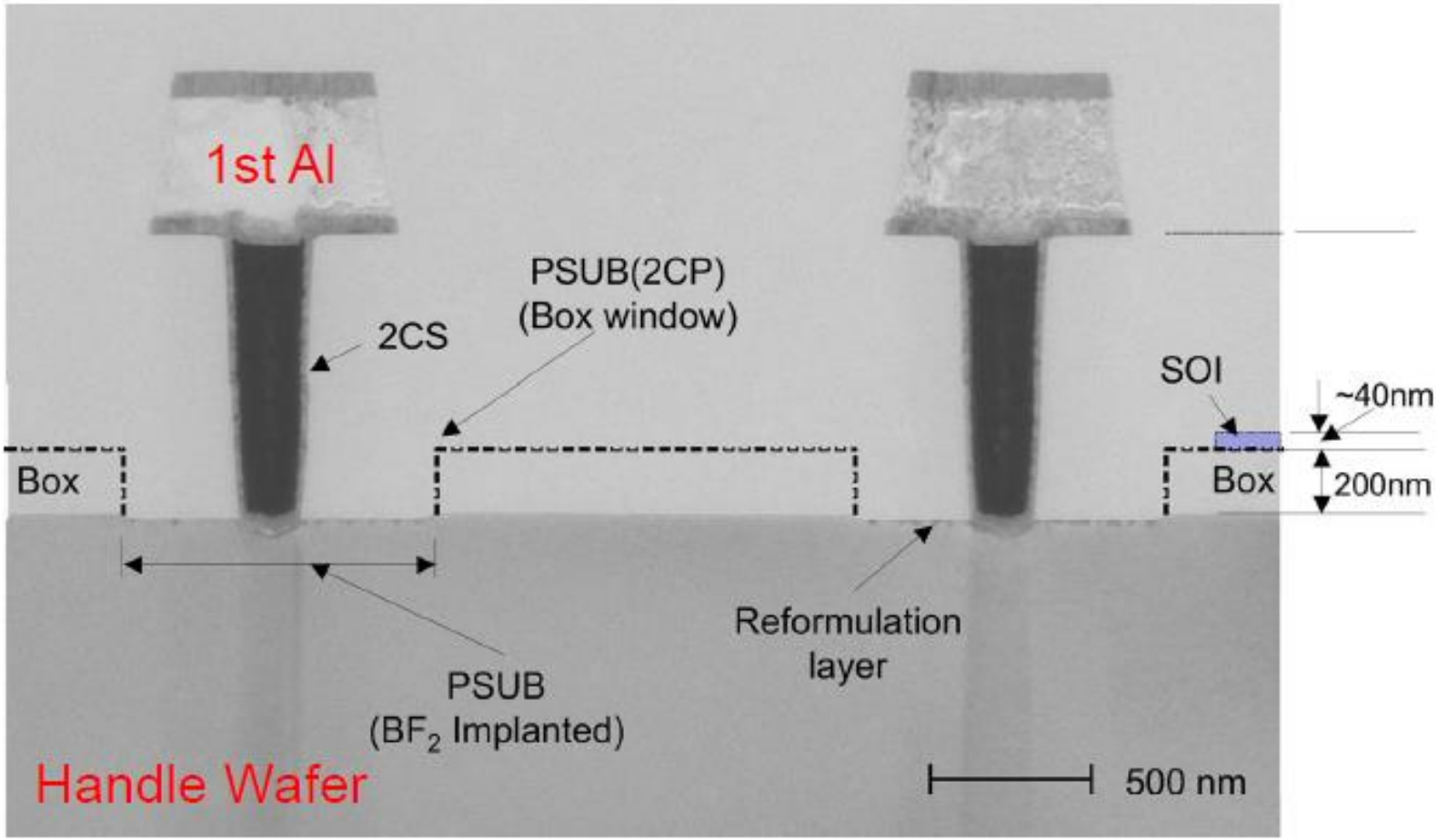


SOI Pixel Process Flow



注意：这是一个为了示例而简化了的工艺流程说明

横截面图（SEM）


1st Al
PSUB(2CP)
(Box window)
2CS
SOI
~40nm
Box
Box
200nm
Reformulation
layer
PSUB
(BF2 Implanted)
Handle Wafer
500 nm

Motivation

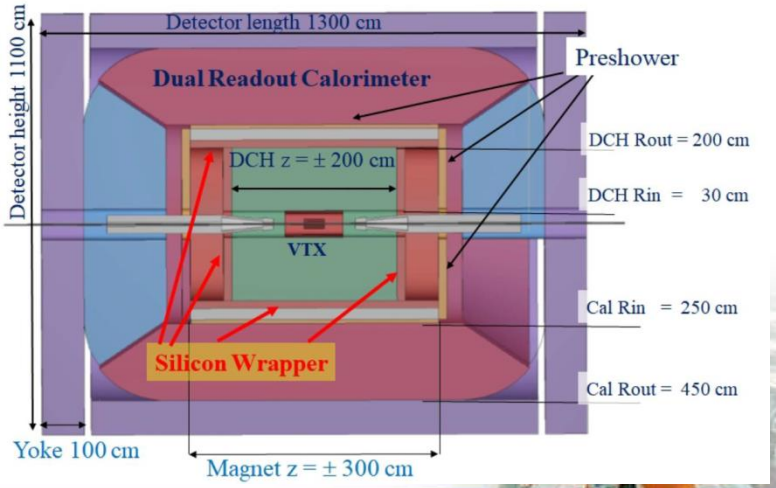
- 高能正负电子对撞实验顶点探测器
  - Identification of heavy quarks (b/c) and τ leptons

$$\sigma_{IP} = a \oplus b/p \cdot \sin^{\frac{3}{2}}(\theta)$$

a与Single point resolution相关

b与带电粒子穿过探测器的Multiple scattering相关

- 对像素探测器的基本要求：
  - 高空间分辨率
  - 低功耗
  - 低物质量
  - 抗辐照损伤



不同类型实验的典型指标比较

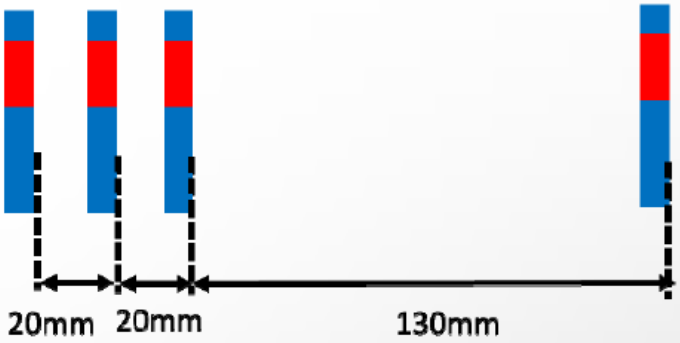
Collider	空间分辨率	功耗	物质量	辐照损伤
PP	7~14um	>200mW/cm^2	0.7% X_0/layer	300 Mrad, 10^{15} n_{eq}/cm^2
Heavy ION	5um	50~200mW/cm^2	0.3% X_0/layer	1 Mrad, 10^{12} n_{eq}/cm^2
e^+e^-	**2.8**um	**50**mW/cm^2	**0.15**% X_0/layer	1 Mrad, 10^{12} n_{eq}/cm^2

INTRINSIC SPATIAL RESOLUTION

- Observed residual spread:σ_{obs}

$$\sigma_{obs} = \sqrt{\sigma_{int}{}^2 + \sigma_{track}{}^2}$$

under an assumption all four FPIXs have the same intrinsic resolution and contributions of misalignment/ multiple scattering are negligible (=conservative σ_{track} value), we can calculate σ_{int} analytically



	1X	2X	3X	4X
Measured residual	0.953 ± 0.009	0.791± 0.008	0.822± 0.008	3.80 ± 0.05
Intrinsic resolution	0.711	0.648	0.703	0.75
	1Y	2Y	3Y	4Y
Measured residual	0.833 ± 0.008	0.683± 0.006	0.824± 0.008	3.79 ± 0.05
Intrinsic resolution	0.622	0.600	0704	0.75

Intrinsic resolution:
0.65~0.71 μm in X
0.60~0.70 μm in Y
(effect of imperfect alignment included)

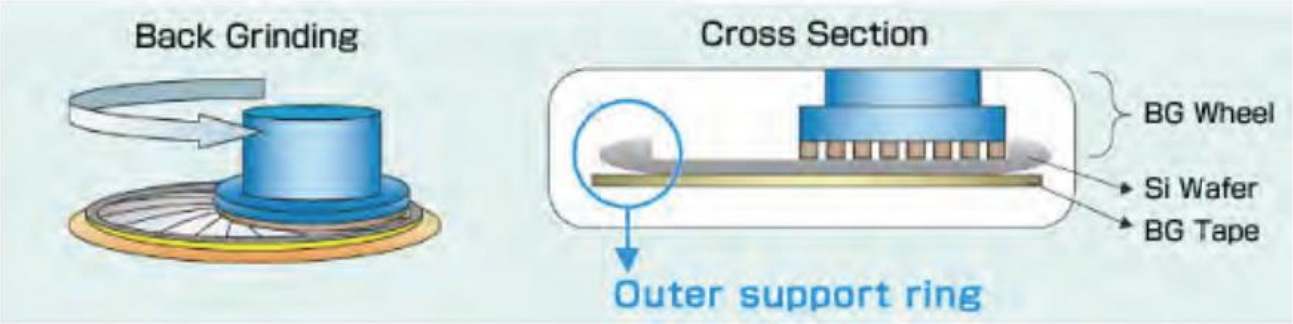
K. Hara, VERTEX2017 Sep 11-15, 2017 Las Caldas

19

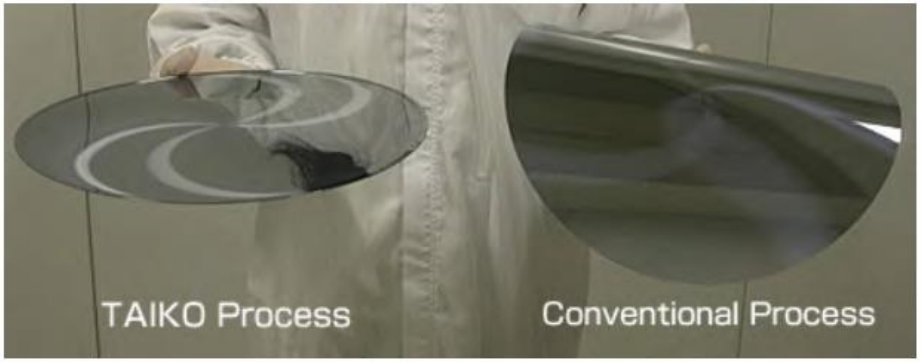
Wafer Thinning

TAIKO Process by DISCO Co.

DISCO
Kiru·Kezuru·Migaku Technologies



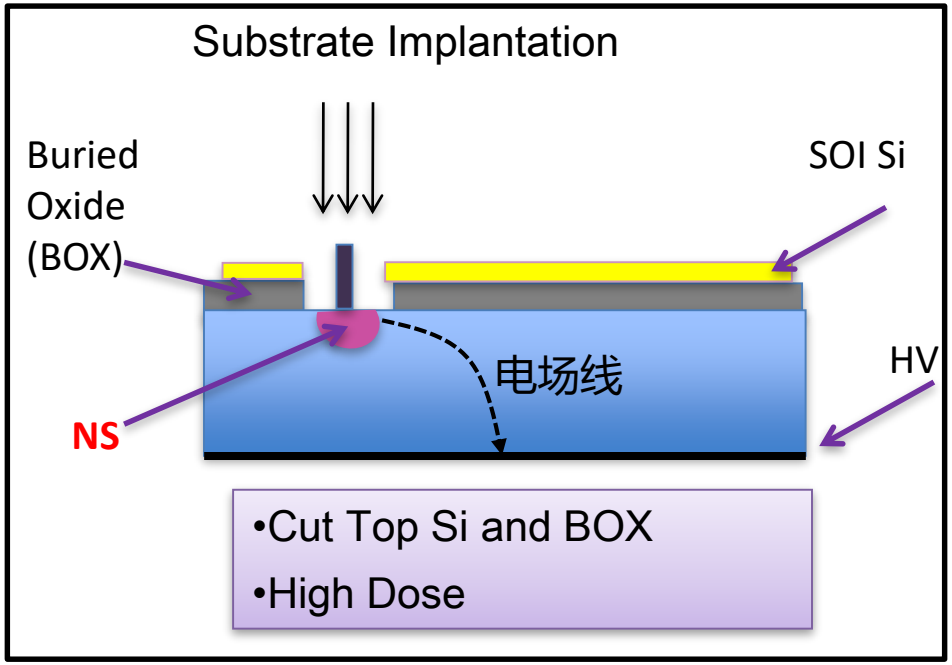
With outer support ring
- Lower wafer warpage
- Improve wafer strength
- Easy wafer handling
- Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning



We have successfully thinned several SOI wafers to ~75 μm thick.

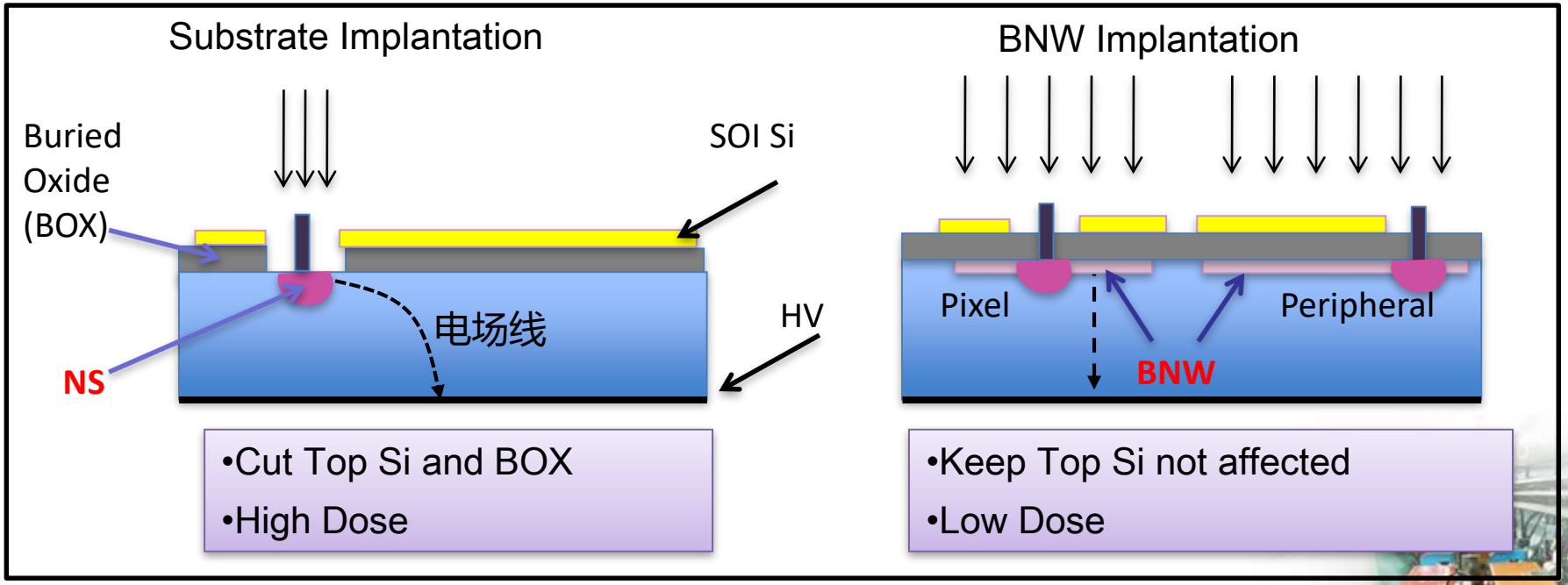
关键技术问题

- Back-gate effect
  - Sensor diode的高压会影响MOS管阈值
  - 高压<10V， 电路与diode距离<7um



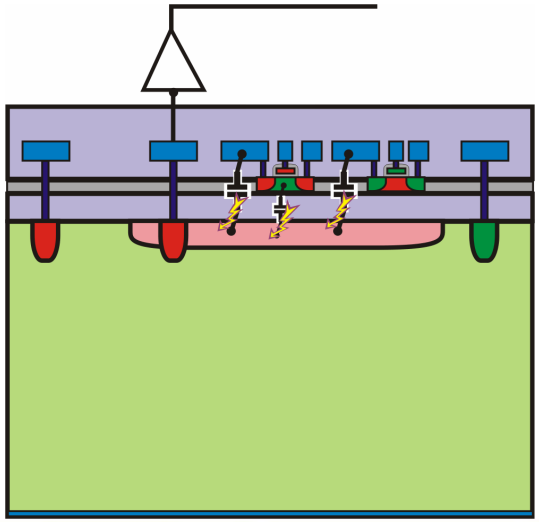
解决方案一：Buried well

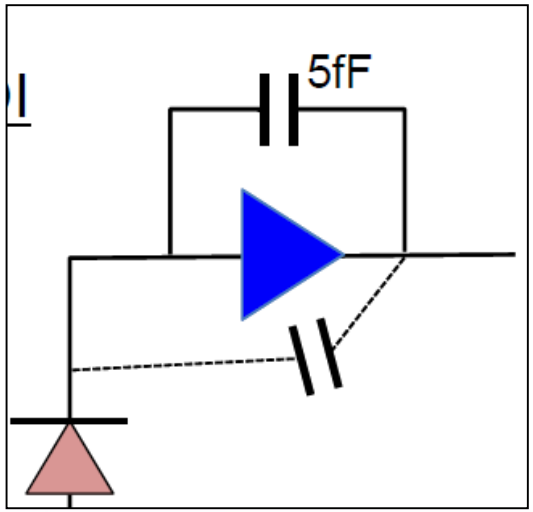
- BNW注入，增大diode面积
  - 背栅电压钳制在Front-end输入电位

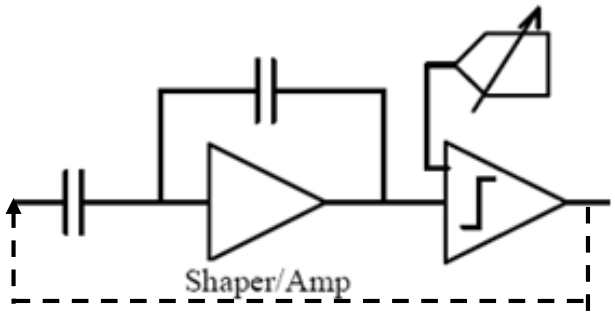


解决方案一： Buried well

- BNW注入，增大diode面积
  - 背栅电压钳制在Front-end输入电位
- 但增加了电容耦合
  - 对于电荷积分型读出，降低增益
  - 对于单脉冲甄别型读出，自激振荡



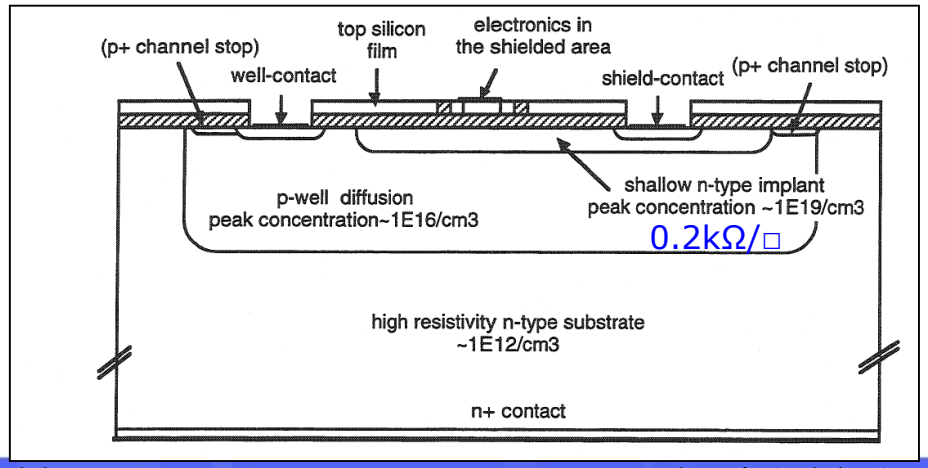




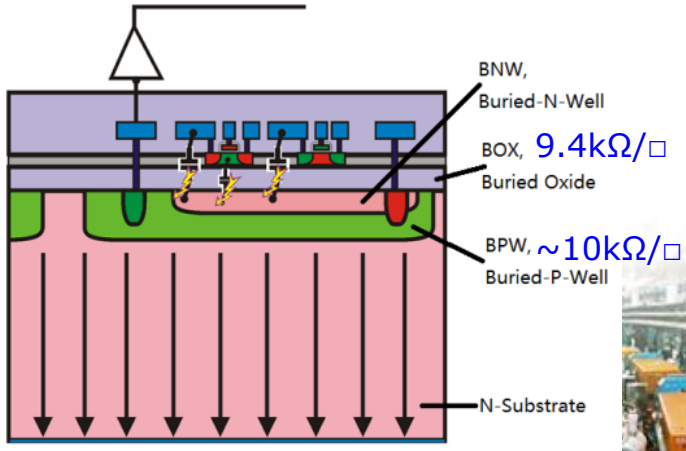
解决方案二： Nested-wells

- P-in-N sensor，BNW作为屏蔽层
  - CERN RD19在1990年代提出但工艺不过关
  - SOIPIX合作组2012年完成了工艺开发

Shielding-well proposed by F. X. Pengg in his dissertation "Monolithic Silicon Pixel Detectors in SOI Technology"



Monolithic Active Pixel Matrix with Binary Counters ASIC with **nested wells**
F. Fahim, Pixel2012



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- 增加了Front-end输入端电容，限制低噪声应用

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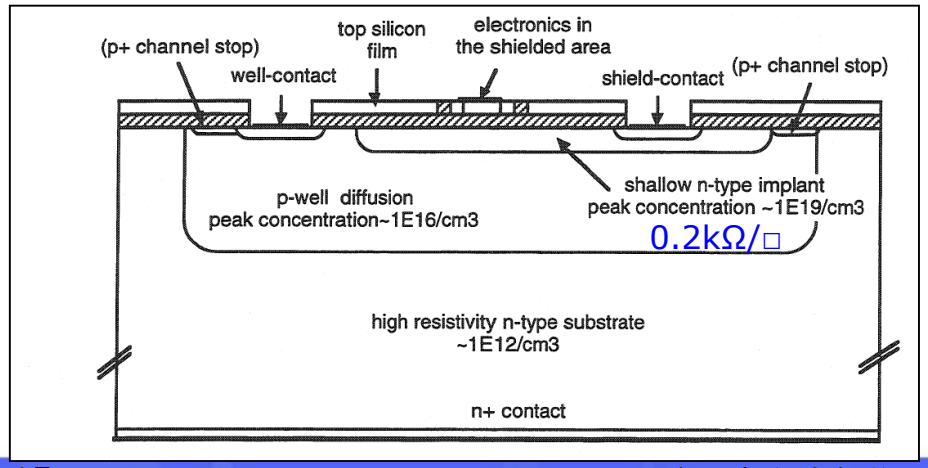

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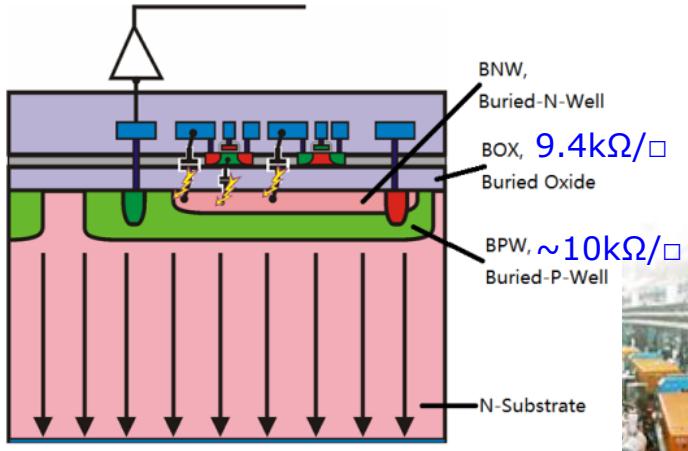
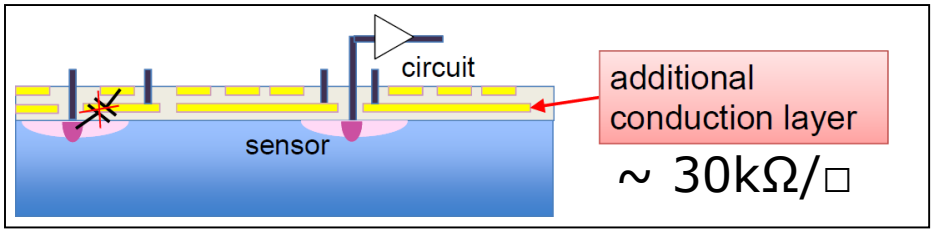
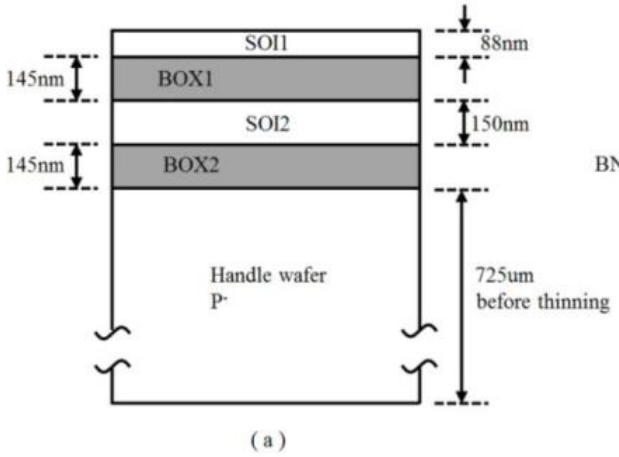
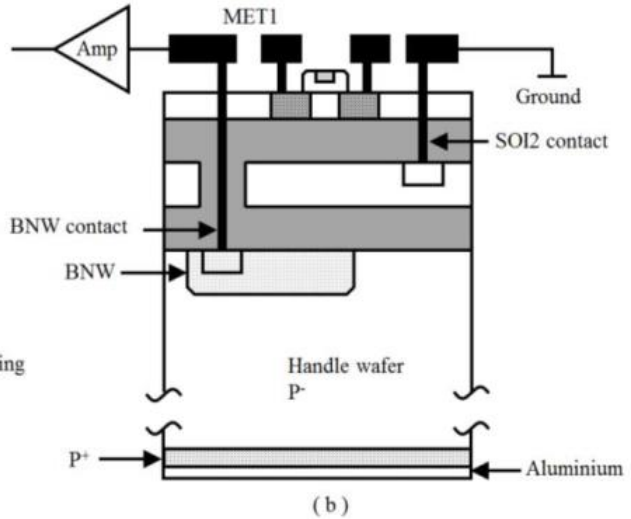


解决方案三： Double-SOI

- 增加一个Device layer作为专用屏蔽层 (SOI2)
  - 阻断电路和sensor diode之间的电容耦合路径
- 并且为MOS管提供独立的背栅电压
  - 解决back-gate effect
  - 补偿TID辐照损伤





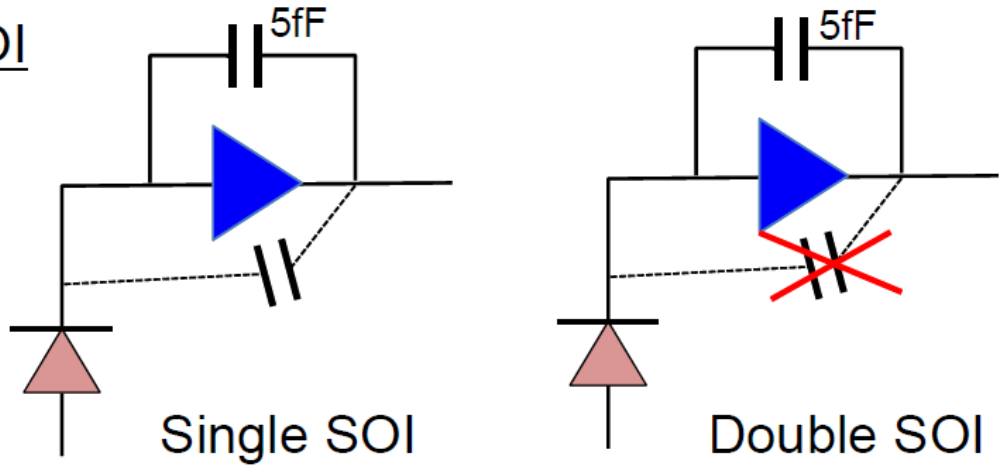


Double-SOI wafer before processing **After processing**

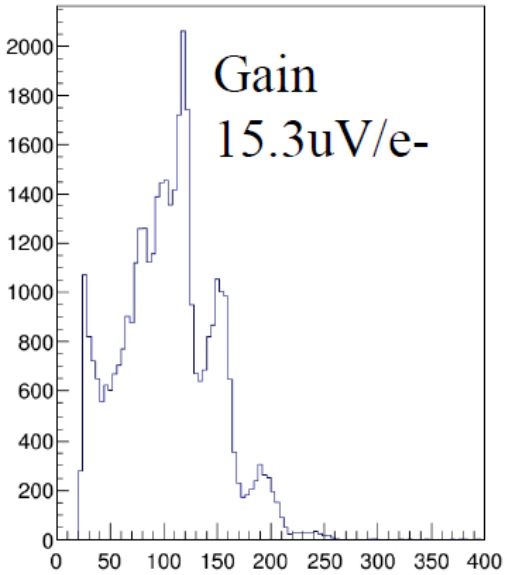
电荷积分型电路测试结果

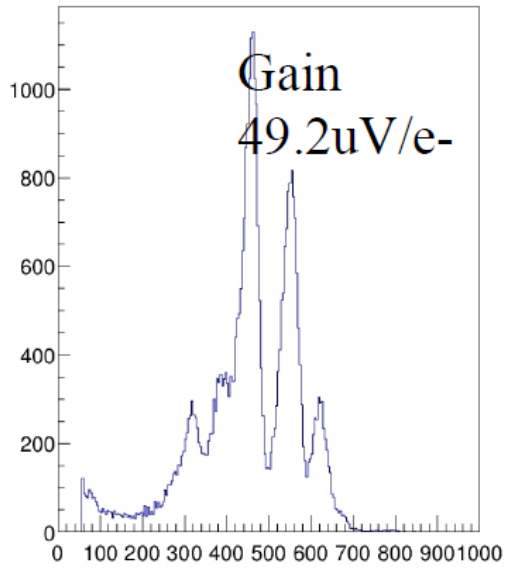
Effect of Double SOI

Coupling:
Gain of Charge Amp increases ~3 times by cutting parasitic C.



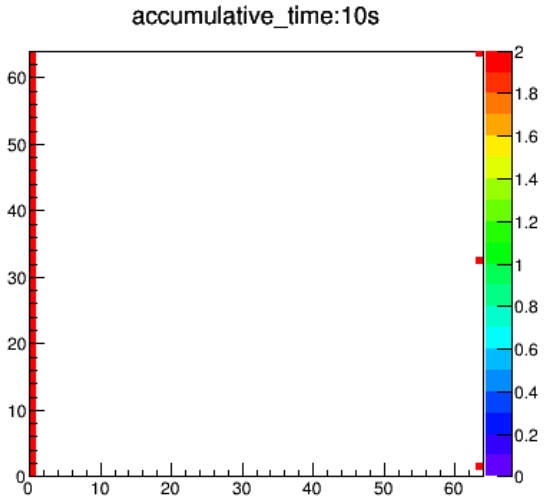
Am241



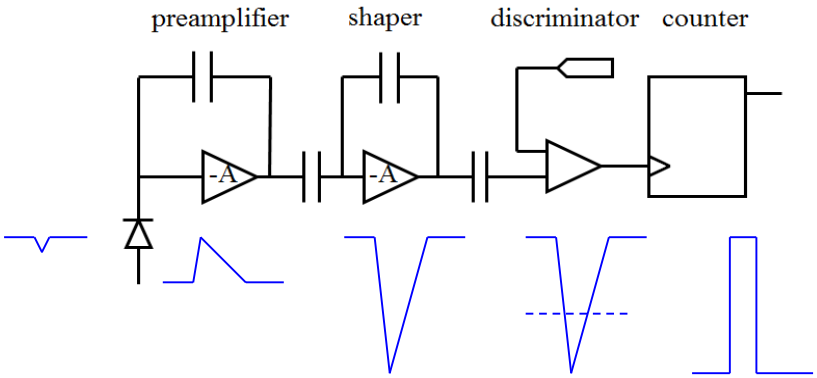


单脉冲甄别型芯片测试结果

- 成功验证了Double-SOI方案：
  - 像素尺寸50*50um^2
  - 阵列规模64*64
  - 阈值: 3keV



1小时内击中3*3*0.15mm^{3}灵敏区的宇宙线事例
计数时间：10s * 360frame = 3600s
芯片竖立放置



Signal processing chain in-pixel

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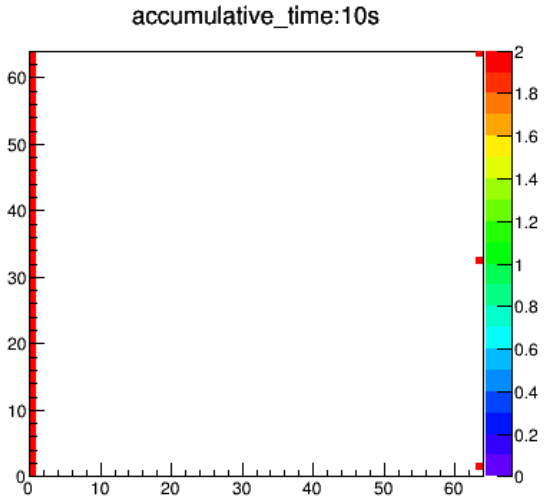

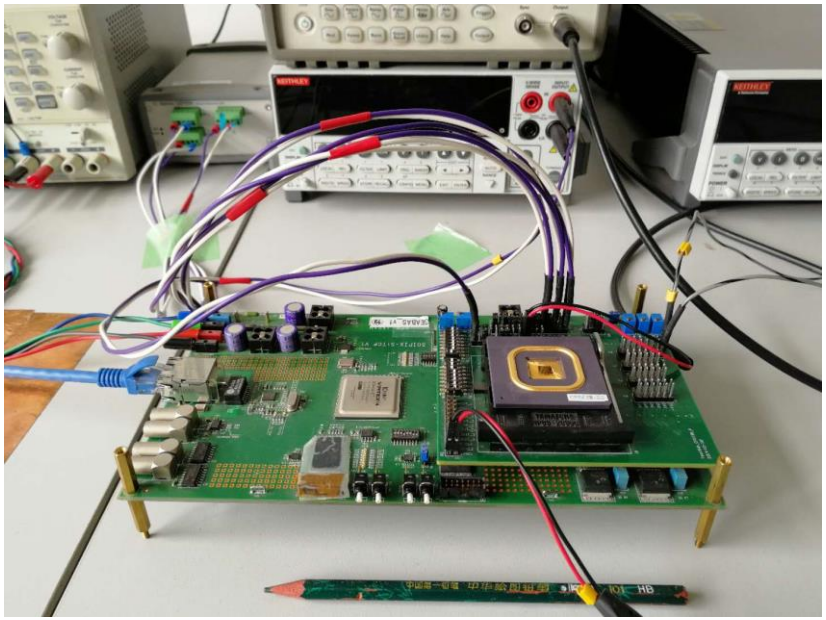

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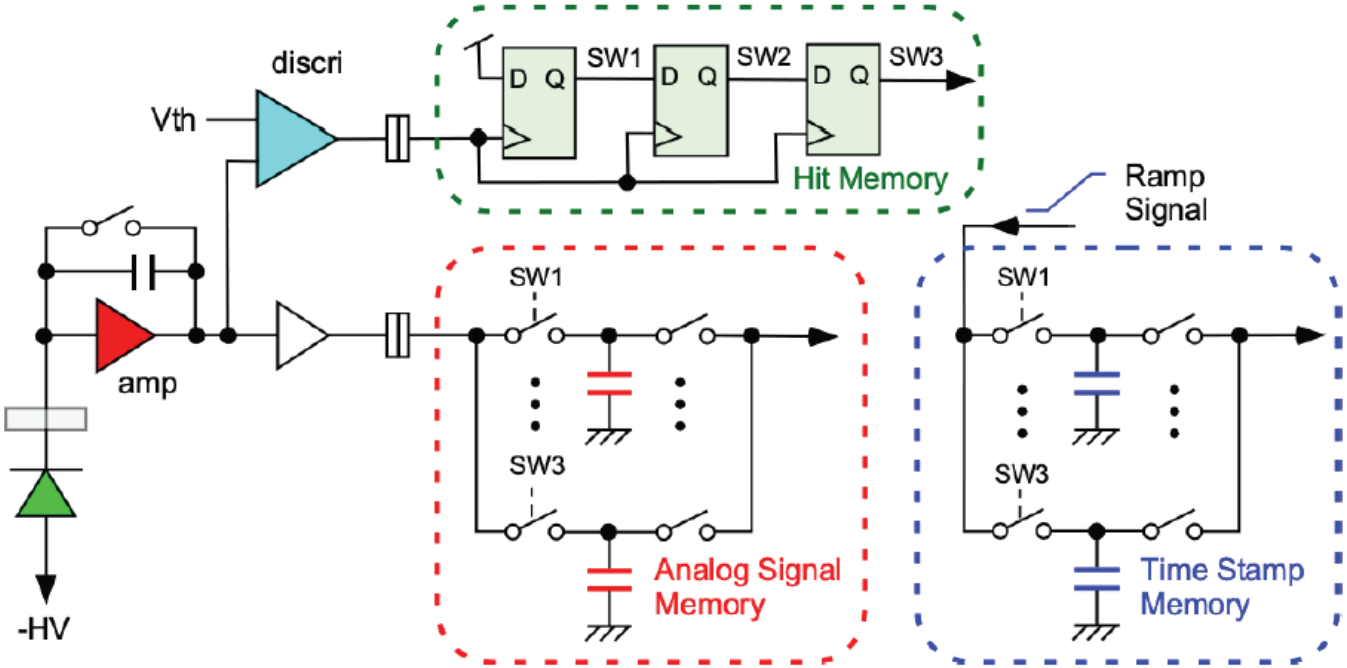
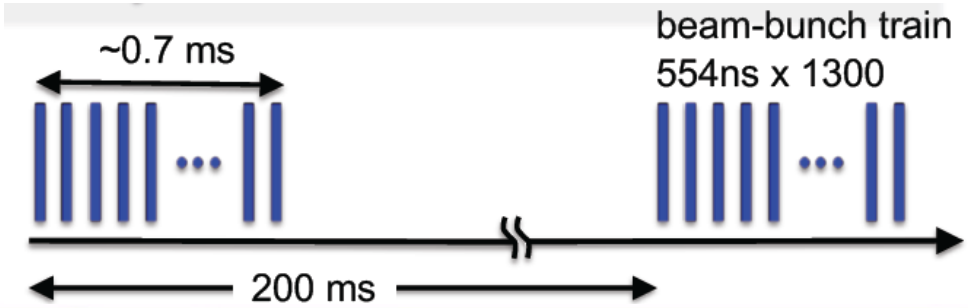
ILC Vertex Detector R&D : SOFIST

(SOI sensor for Fine measurement of Space & Time)



ILC beam timing



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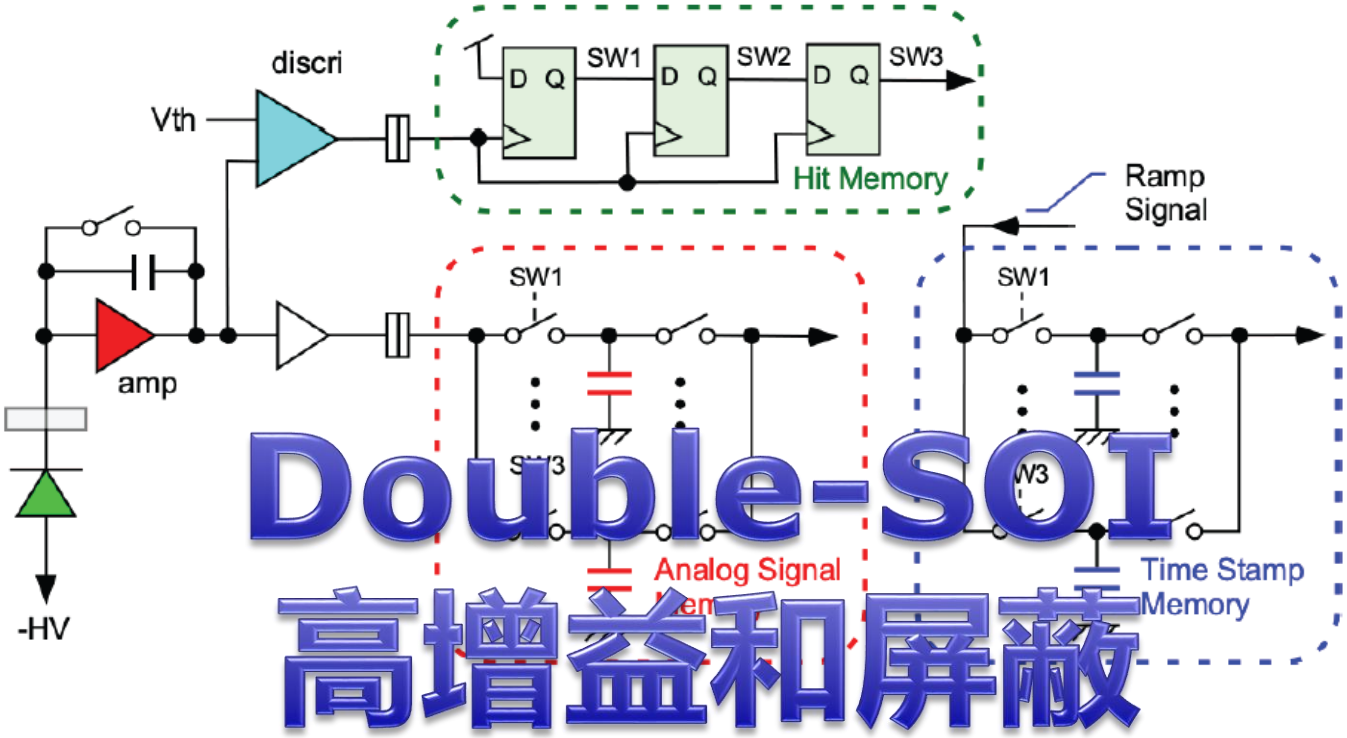

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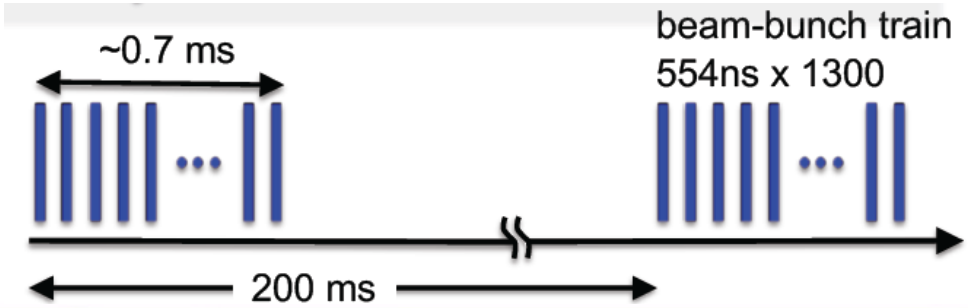


Position Resolution

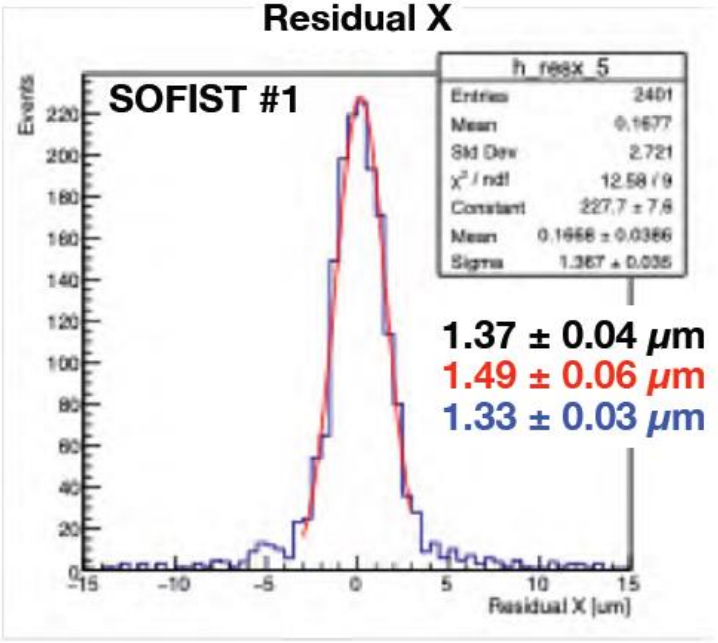
SOFIST Ver. 1

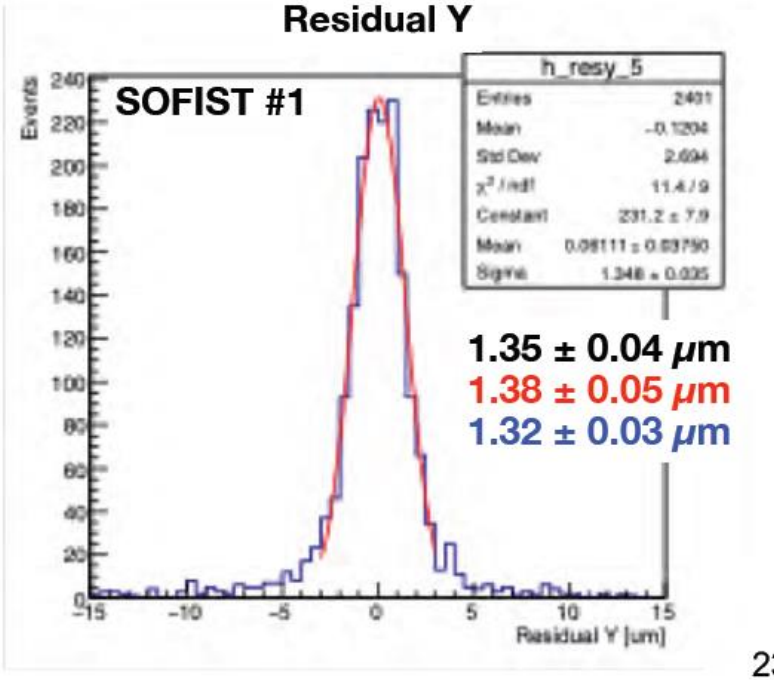
Readout and Sensor depletion layer

12-bit external ADC, 500 μm (Full depletion)

8-bit on-chip ADC, 500 μm (Full depletion)

12-bit external ADC, 200 μm (Partial depletion)



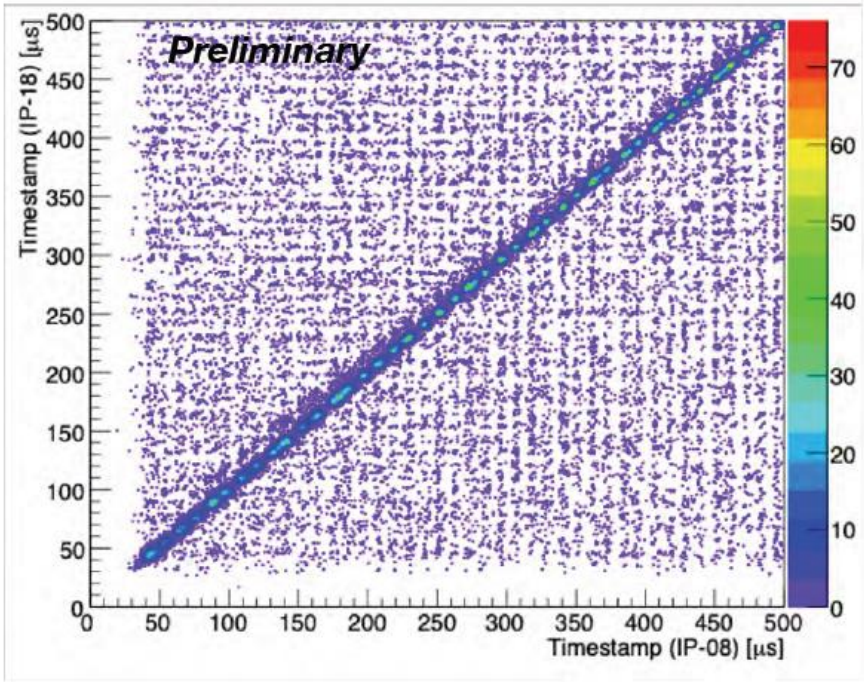


23

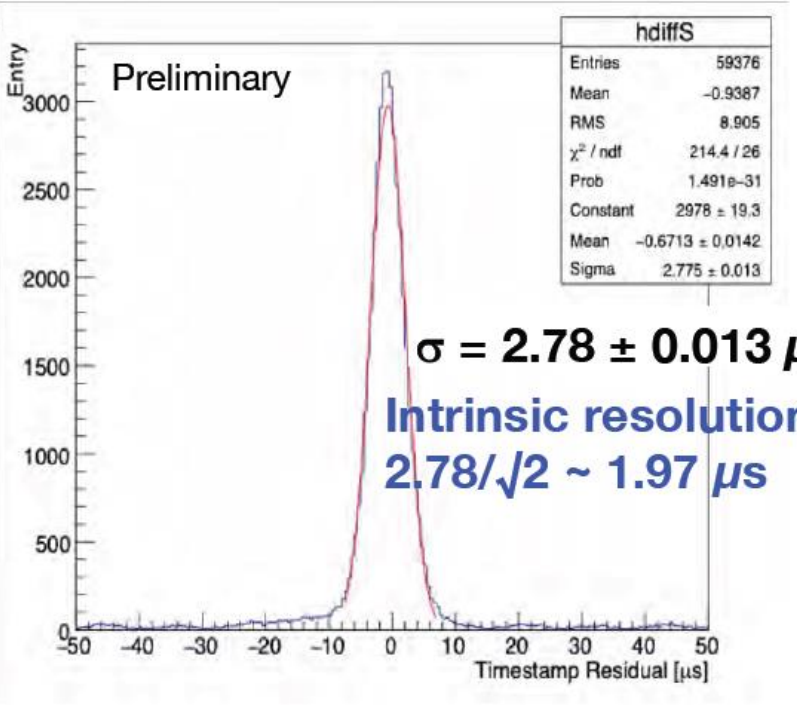
Time Resolution

SOFIST Ver.2

Timestamp correlation between SOFIST ver.2 #1 and #2



Timestamp residual between SOFIST ver.2 #1 and #2



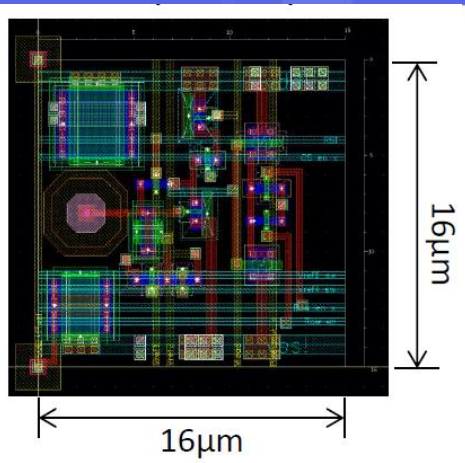
σ = 2.78 ± 0.013 μs

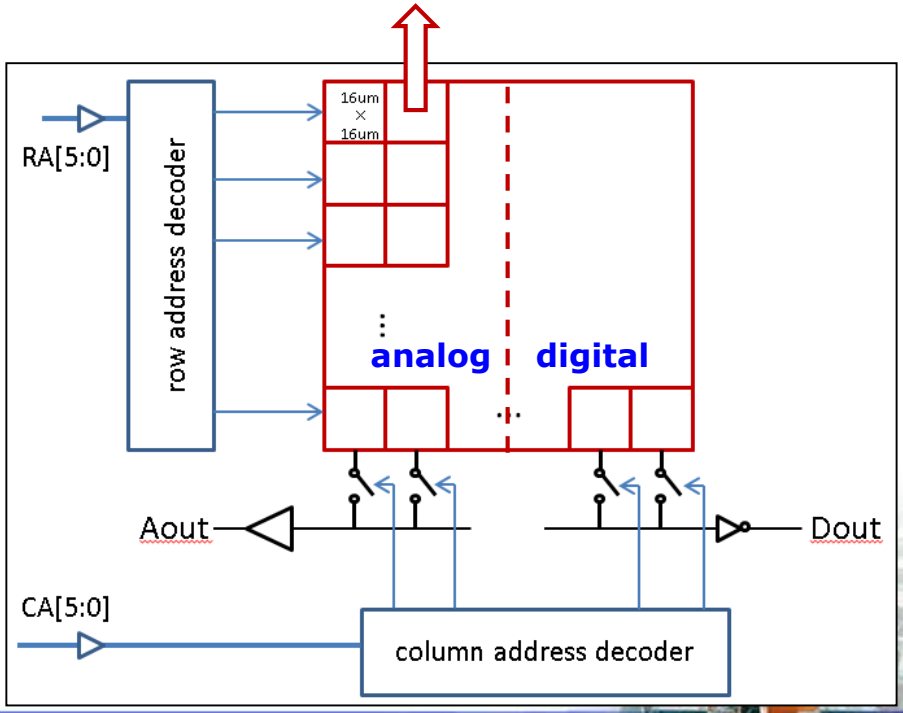
Intrinsic resolution: 2.78/√2 ~ 1.97 μs

Bench test resolution is about 1 μsec.

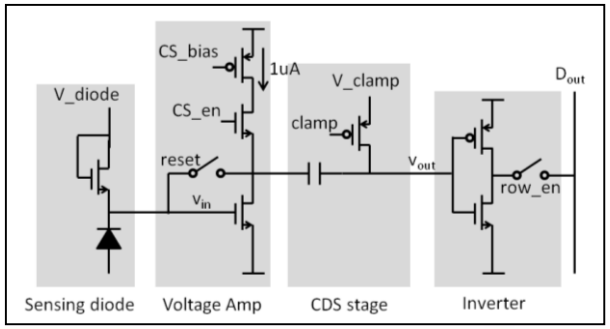
CPV Chip architecture

- CPV (Compact Pixel for Vertex)
  - Pixel size: 16 × 16 μm^2
- Pixel circuit
  - Sensing diode, amplifier, discriminator
- Rolling shutter mode
  - 100 ns / row
- 64 rows × 64 columns
- Thinned down to 75um





Pixel circuit in CPV2



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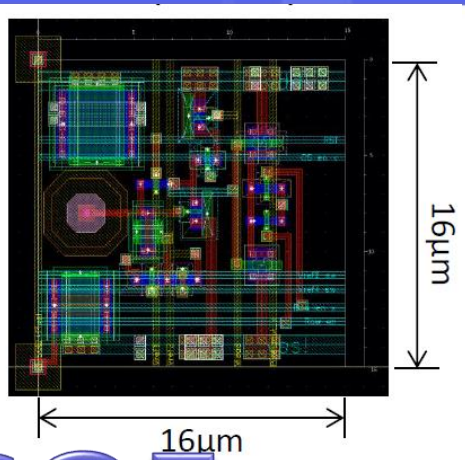
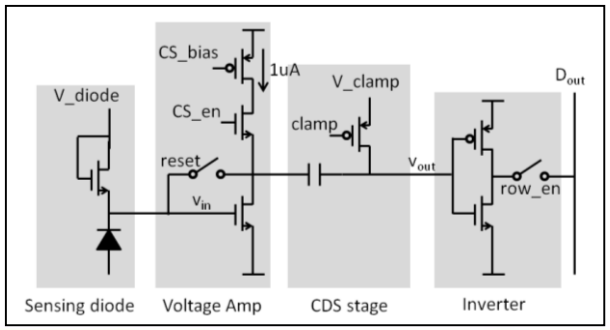
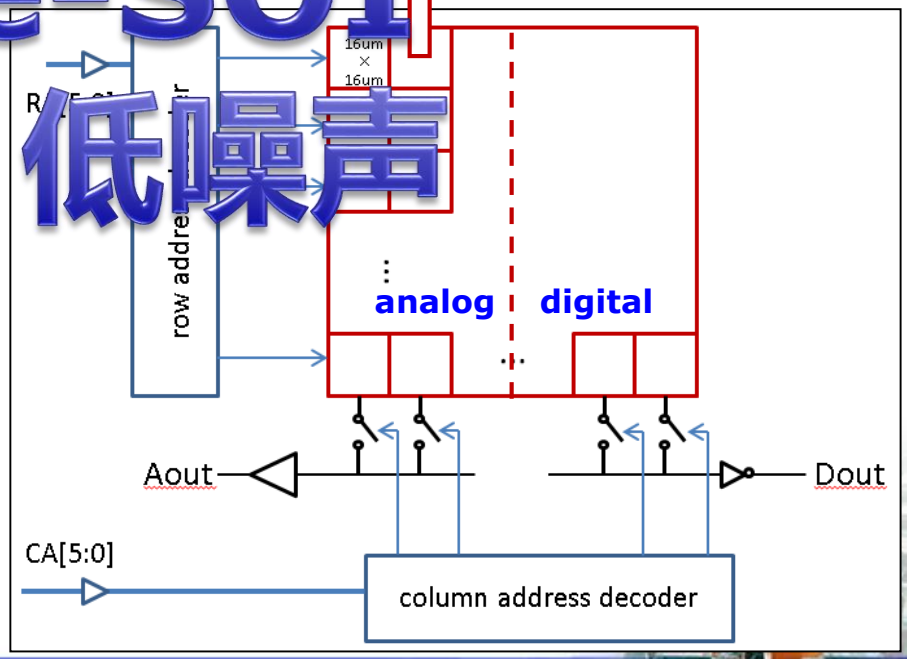
  - Pixel size: 16 × 16 μm²
- Pixel circuit
  - Sensing diode, amplifier, discriminator
- Rolling shutter mode
  - 100 ns / row
- 64 rows × 64 columns
- Thinned down to 50 μm



Double-SOI
高增益，低噪声

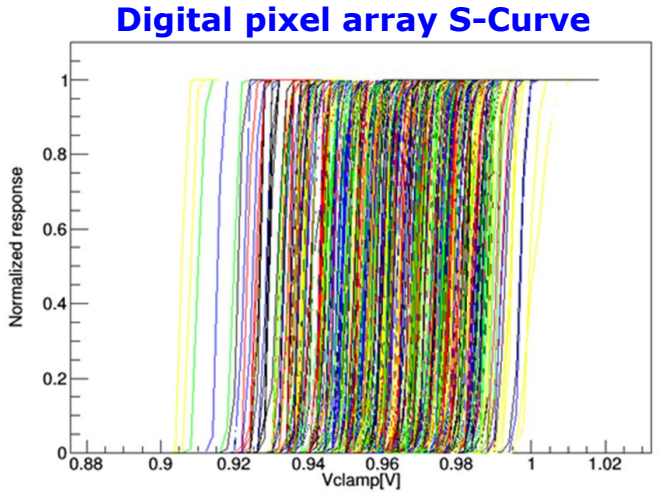
Pixel circuit in CPV2

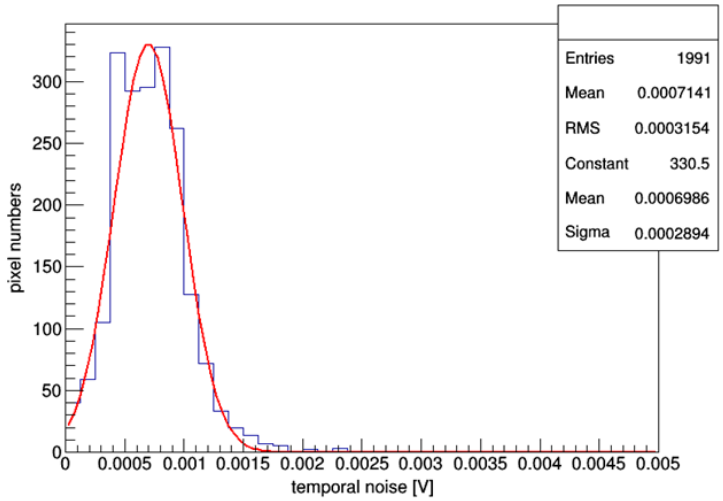


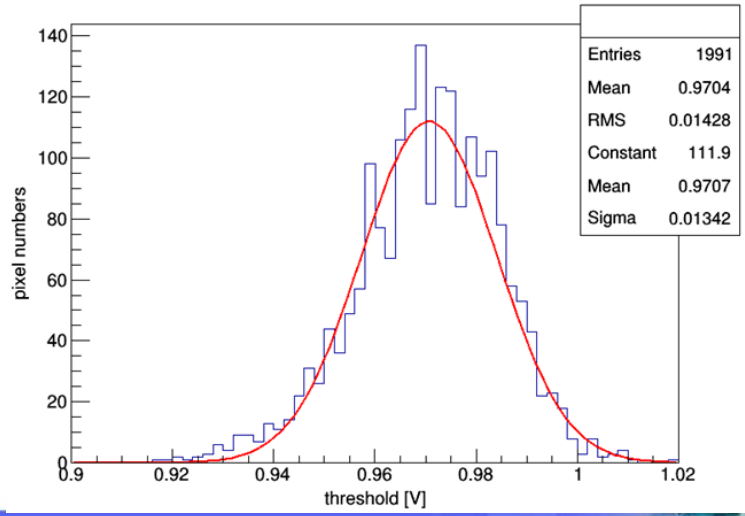


Noise Measurement

- S-curve measured on the digital pixel array
  - 瞬态噪声 ~ 6 e^-
  - 阈值分布 ~ 114 e^-

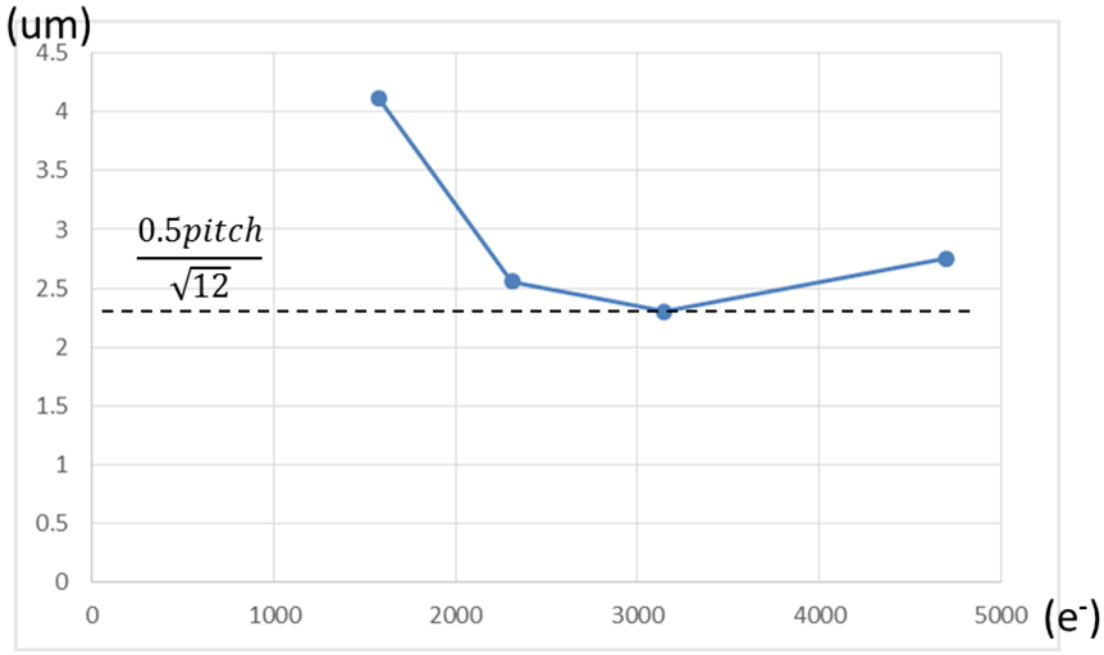






Single Point Resolution

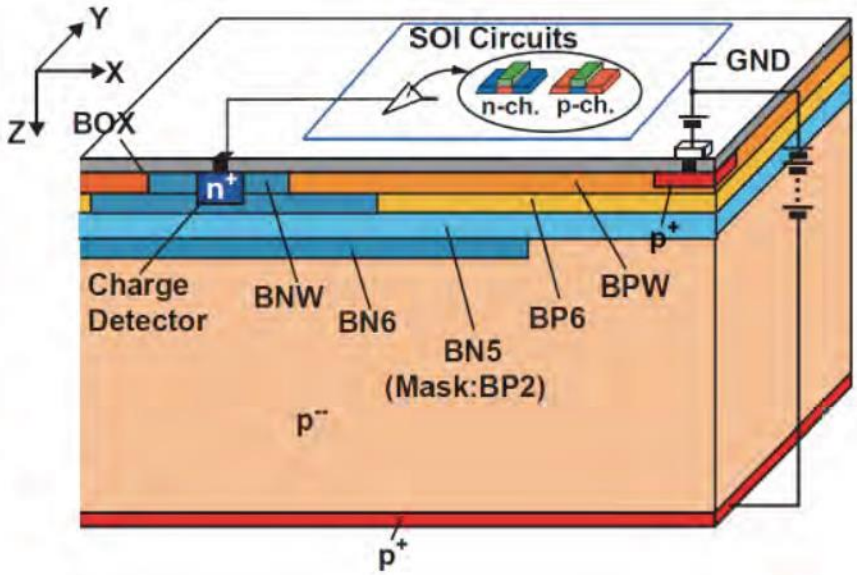
- Single point resolution versus signal charge
  - Obtained the best resolution of 2.3um around signal charge 3000 e^-
  - Low threshold is critical

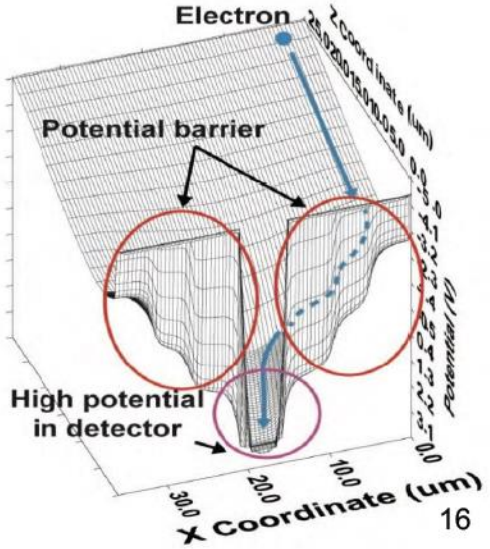


SOI技术展望

New Sensor Structure:
Pinned Depleted Diode
(SOIPIX-PDD)

1、降低对定制Double-SOI晶圆的依赖程度
2、降低常温下Dark Current两个量级
3、降低大面积电荷收集极的Cd，有利于低噪声应用





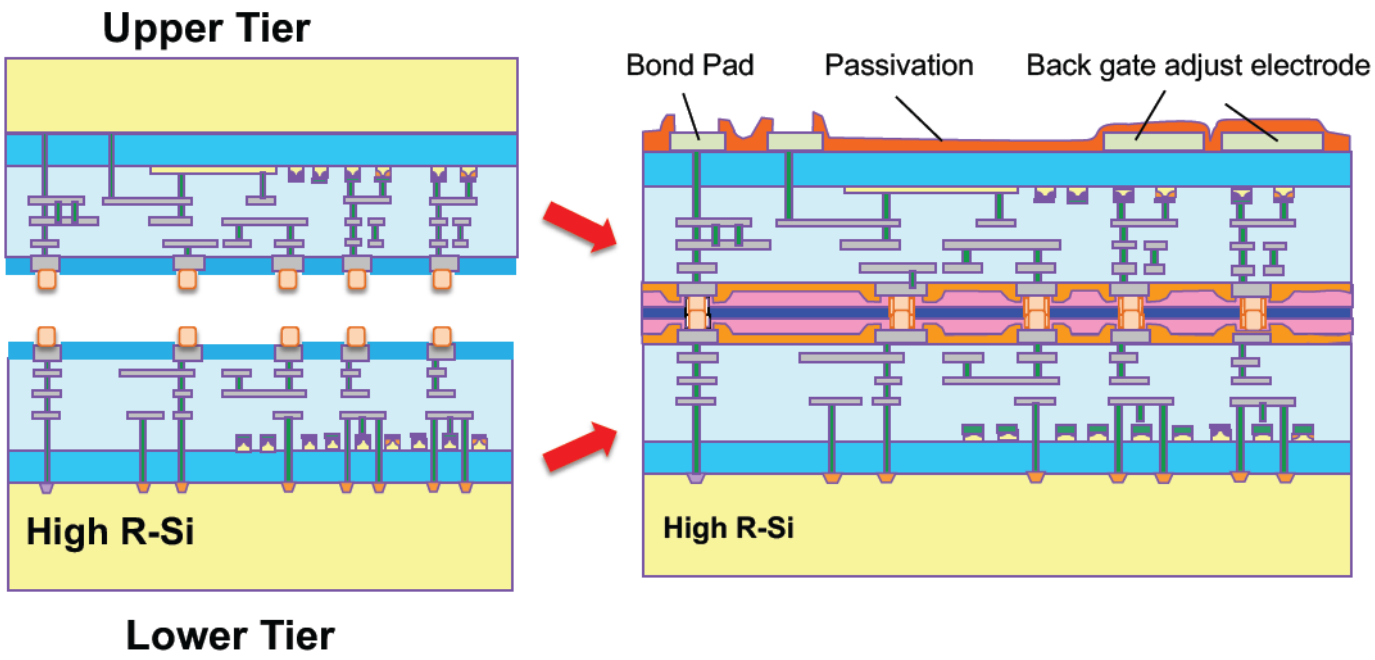
(Shizuoka U., Prof. Kawahito)

SOI技术展望

3D Integration

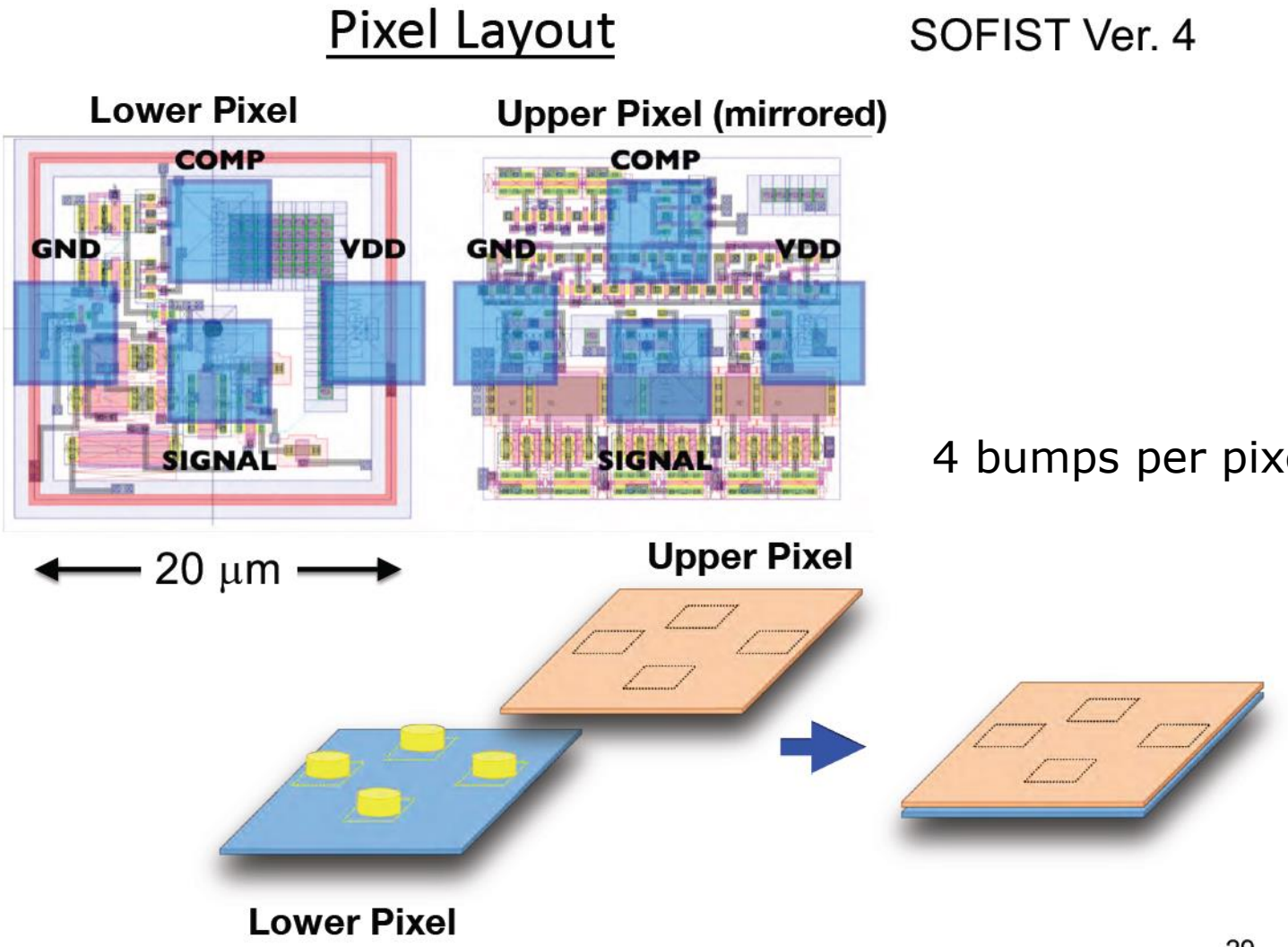
SOFIST Ver. 4

T-Micro



Upper and Lower Tier chips are produced in a same wafer and bonded chip to chip.

SOI技术展望

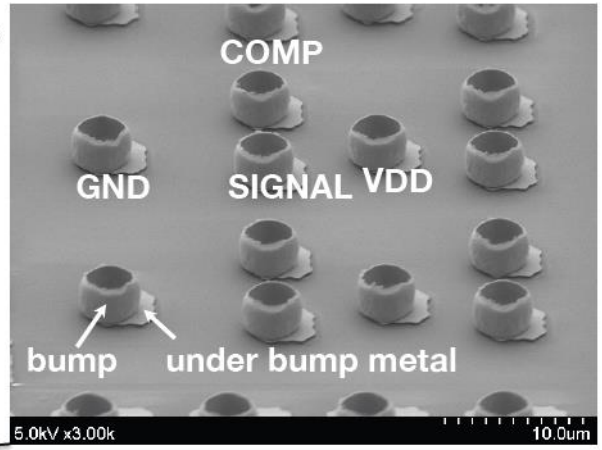

Pixel Layout
SOFIST Ver. 4
Lower Pixel
Upper Pixel (mirrored)
COMP
GND
VDD
SIGNAL
COMP
GND
VDD
SIGNAL
20 μm
Upper Pixel
Lower Pixel
4 bumps per pixel
29

SOI技术展望

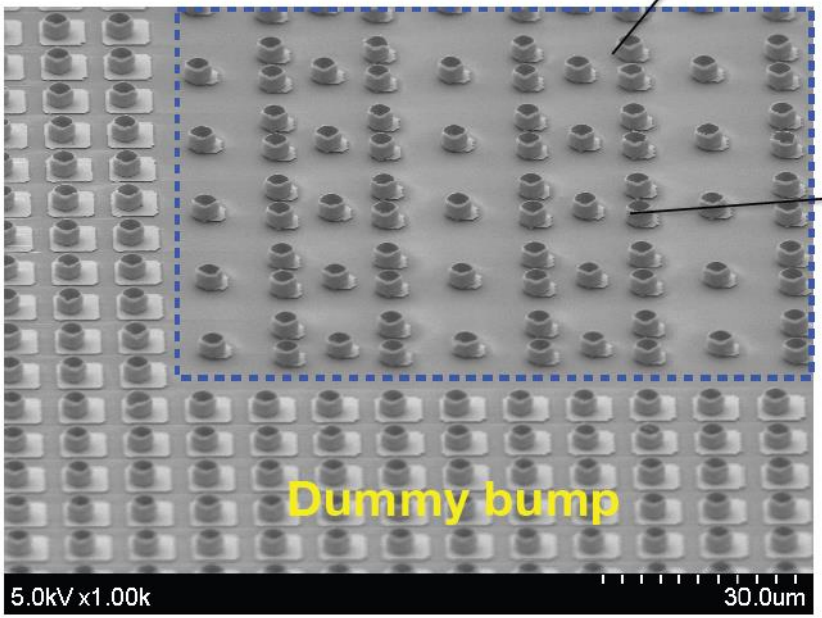
SOFIST Bump

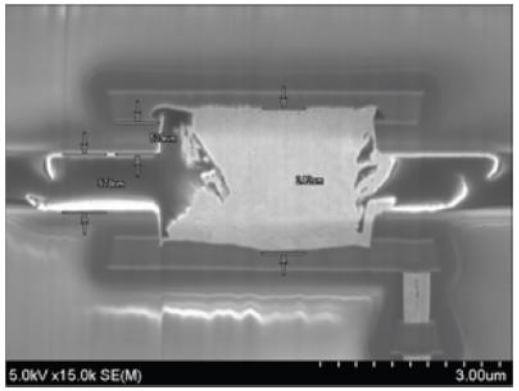
Cylinder bumps are successfully fabricated

Pixel



Pixel array





3D SOFIST will be tested soon.

32

总结

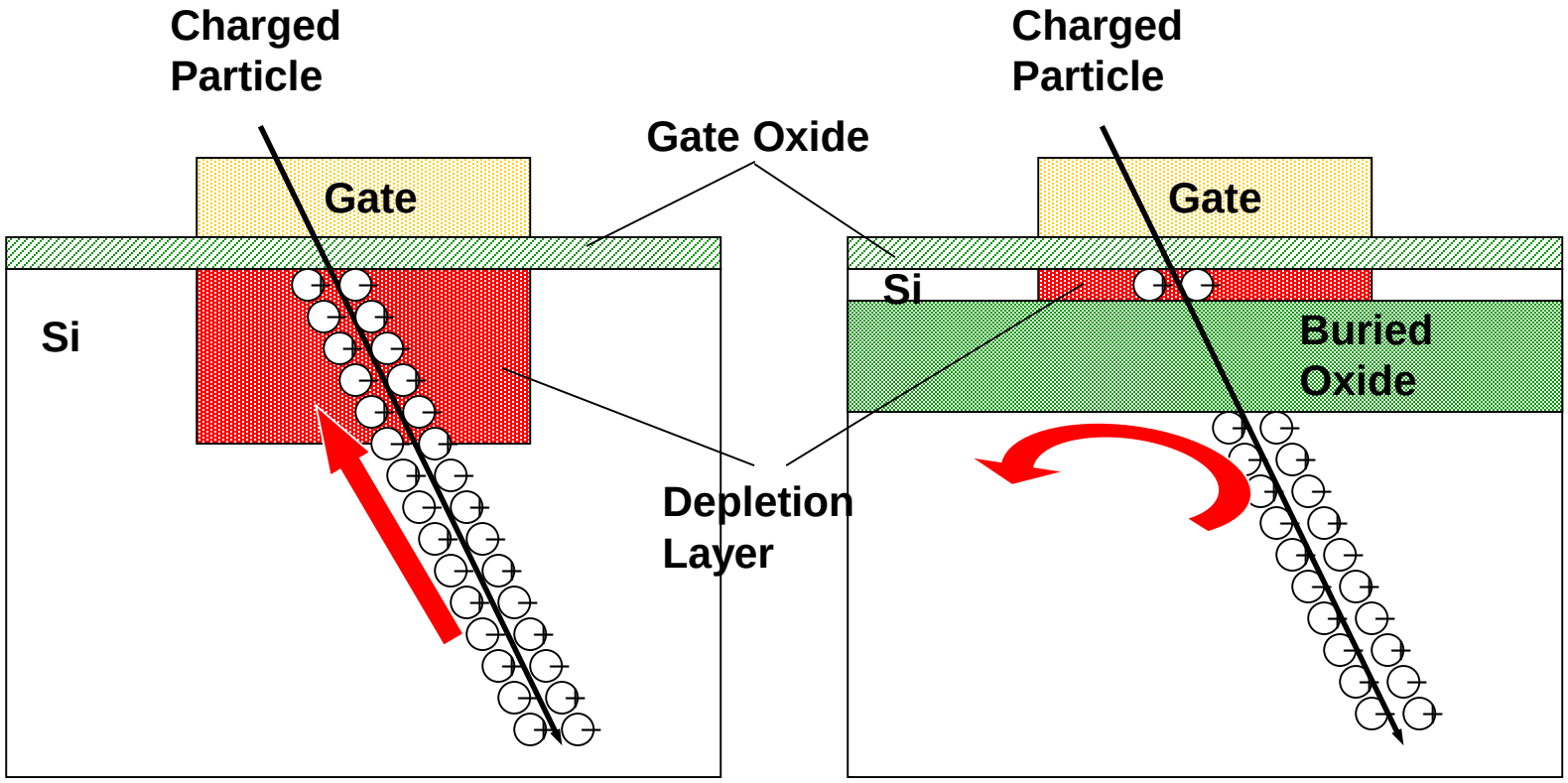
- SOI像素探测器的发展经历了长期的过程
  - 与Foundry之间密切合作
- 针对不同的实验需求，提出了芯片的优化方案
- SOIPIX的更多信息请查阅：
  http://rd.kek.jp/project/soi/

致谢

- 感谢KEK的Yasuo Arai, Toru Tsuboyama, Shun Ono, Miho Yamada提供SOFIST和3D相关的内容!
- 感谢重点实验室历年对SOI像素探测器研究的支持!

Backup slides

Single Event Effect

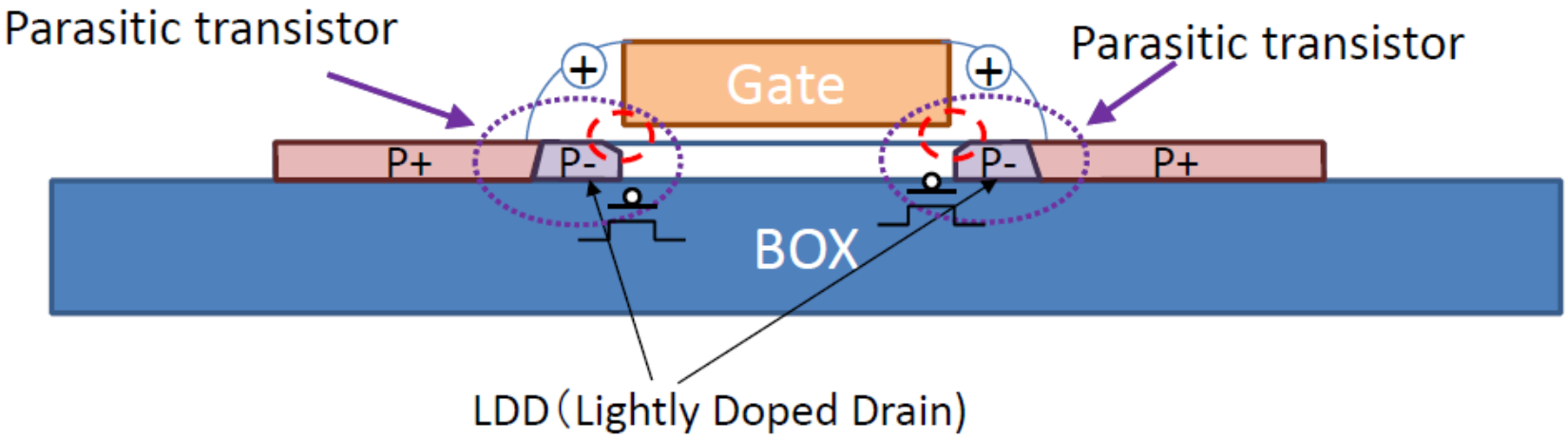


Bulk Device

SOI Device

Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation by radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



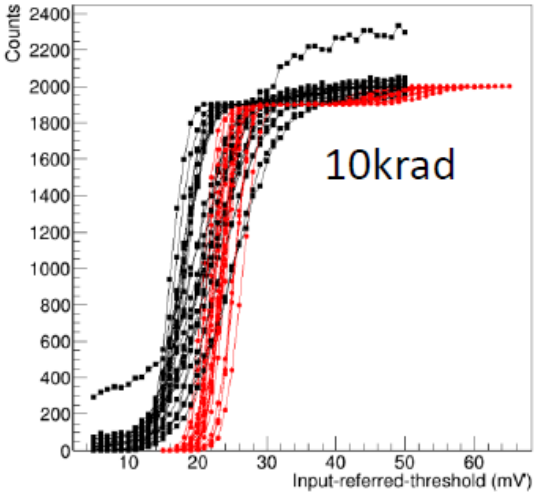
(by I. Kurachi)

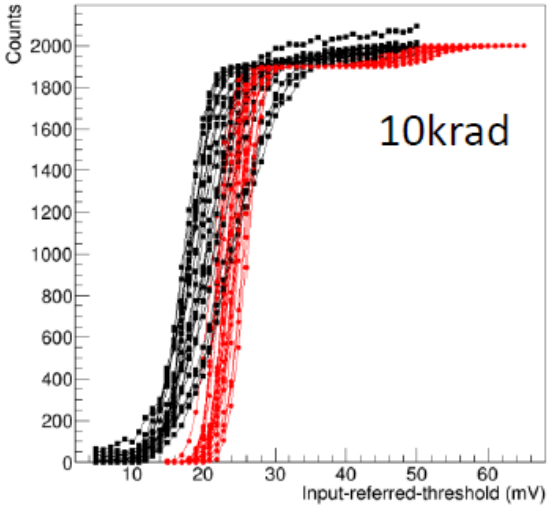
TID compensation in SOI2

- 16 pixels in the center of irradiated area were selected
- Pulse scan
  - Threshold set to 1304mV (corresponds to 24mV of input pulse)

Black: SOI2 0V
Red: SOI2 -0.6V

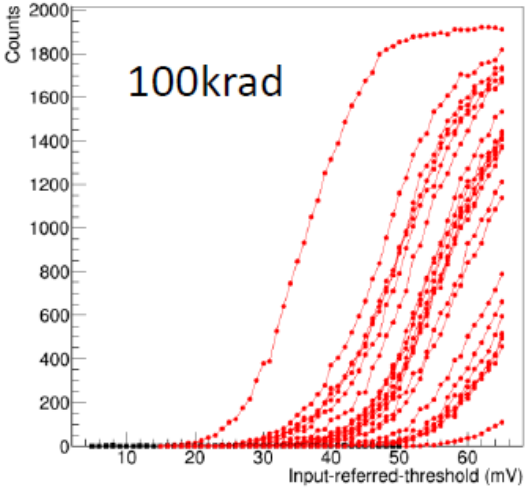
The compensation effectiveness was obvious.

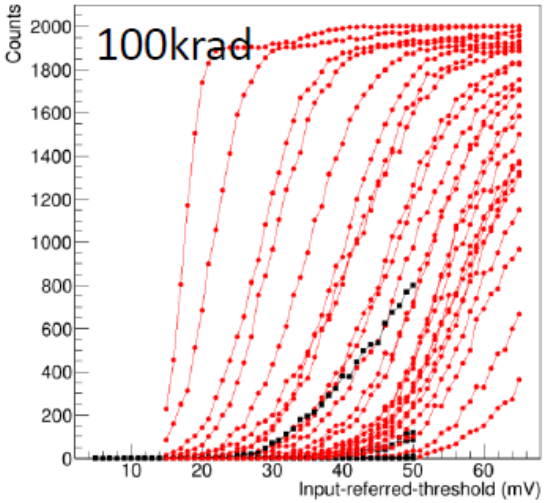




w/o P-spray

w/ P-spray





Occupancy at the first Vertex layer

Operation mode	H (240)	W(160)	Z (91)
Hit density (hits $\cdot$ cm^{-2} $\cdot$ BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

Here we assume **10 μs of readout time** for the silicon pixel sensor and an average cluster size of 9 pixels per hit, where a pixel is taken to be 16×16 μm^2. The resulting maximal occupancy at each machine operation mode is below 1%.