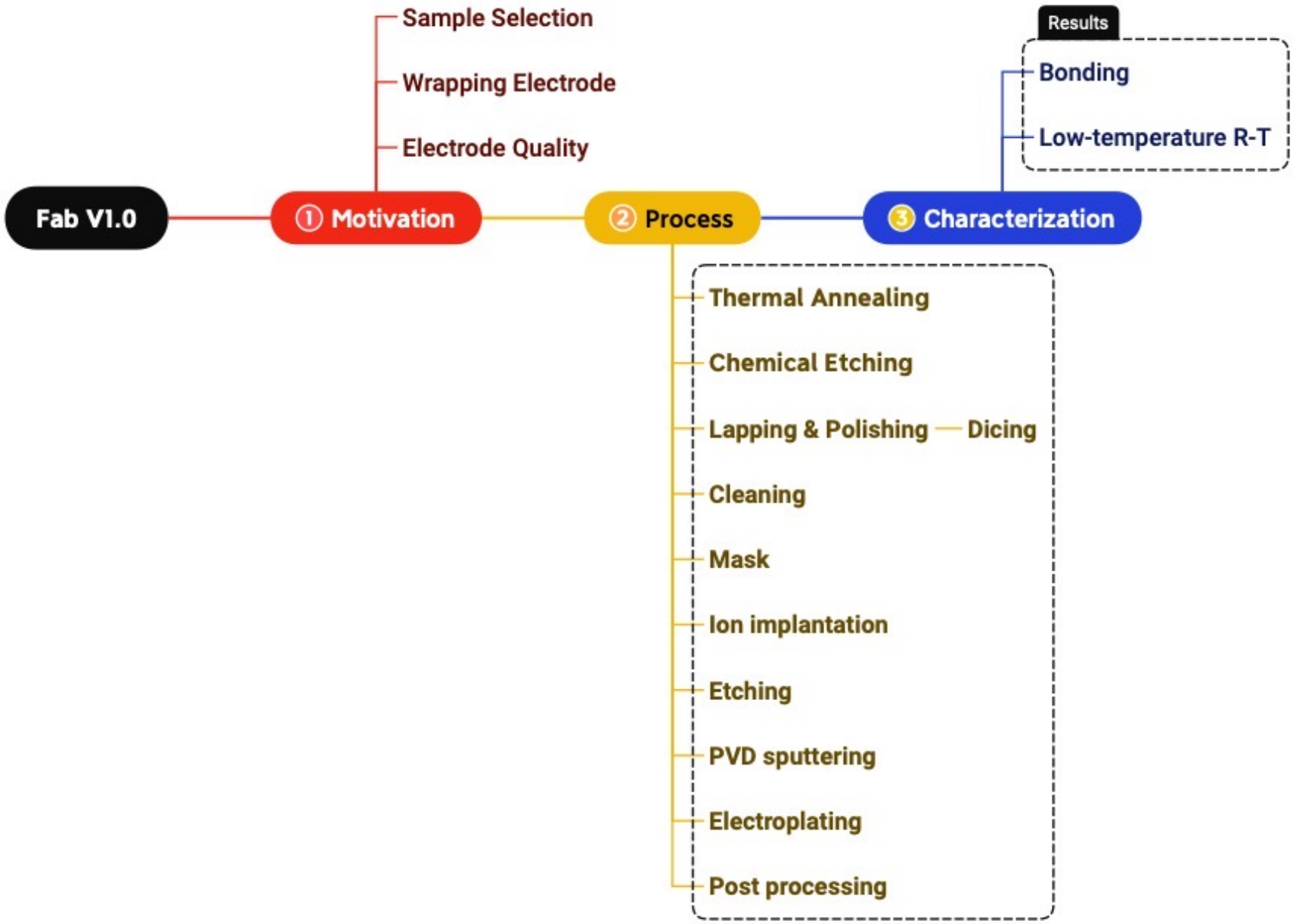
NTD-Ge Fabrication

Kangkang Zhao

2023/08/02

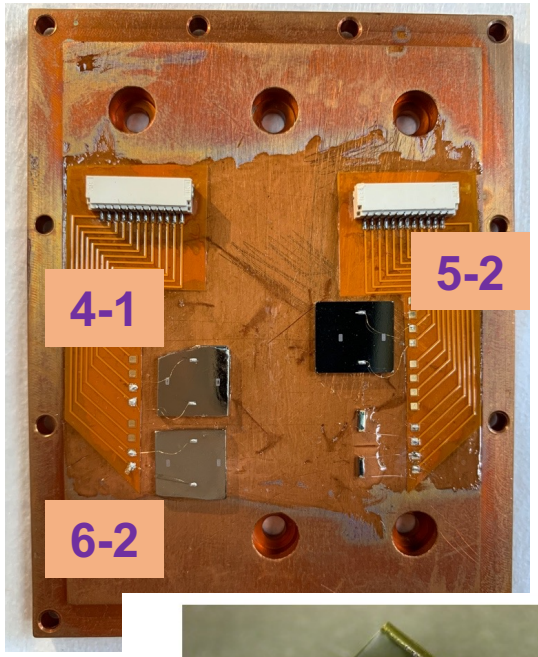
Technological process

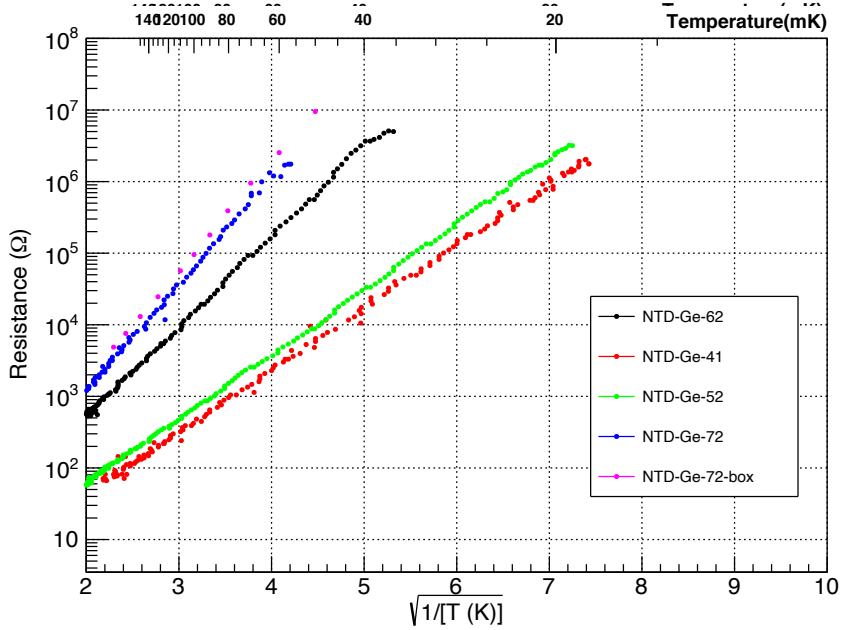


- Sample Selection
- Wrapping Electrode
- Electrode Quality

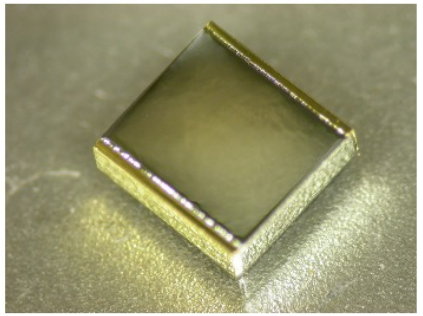
① Motivation

选择两片加工?
1片 10mm*10mm
3片 10mm*3mm





Sample	R0	T0
7-3	1.27	11.72
6-2	1.53	8.45
5-2	1.08	4.16
4-1	0.77	4.04



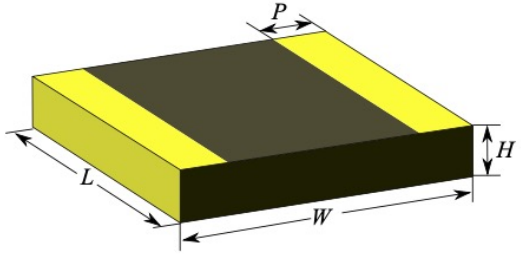
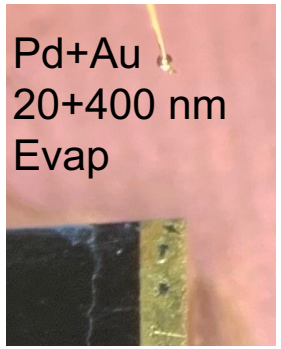
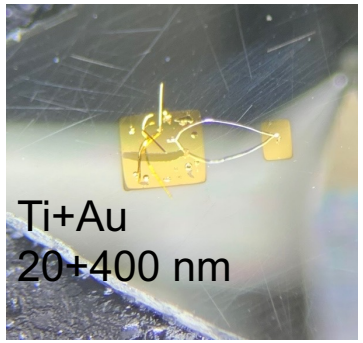
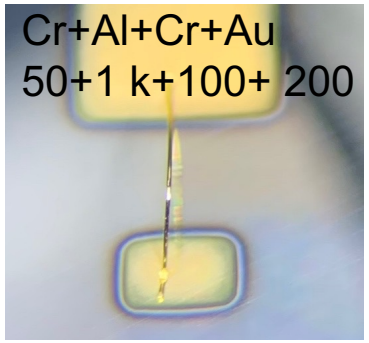
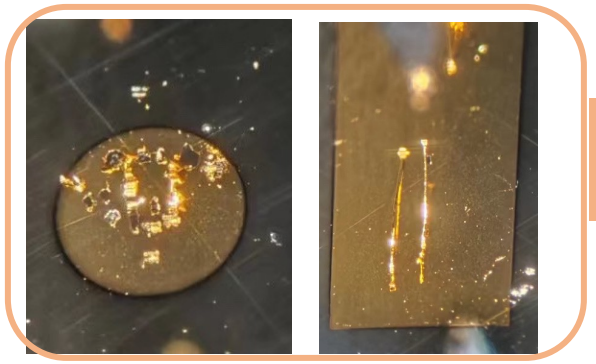


Figure 4. Left: photograph of a CUORE-0 thermistor. Right: diagram of the wrap-around thermistor geometry. Typical values for the dimensions are $L = 3.0$ mm, $W = 2.9$ mm, $H = 0.9$ mm and $P = 0.2$ mm.





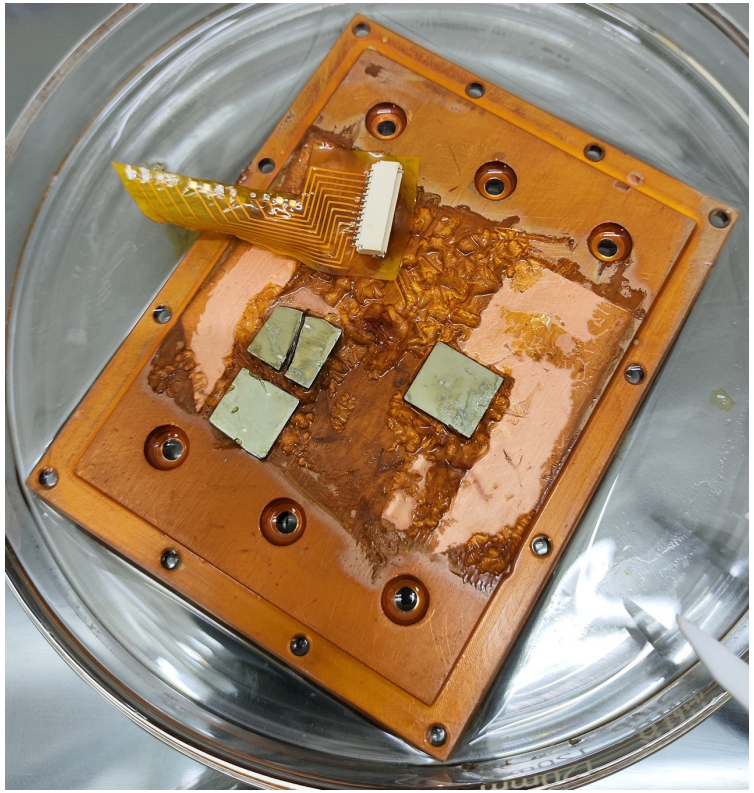


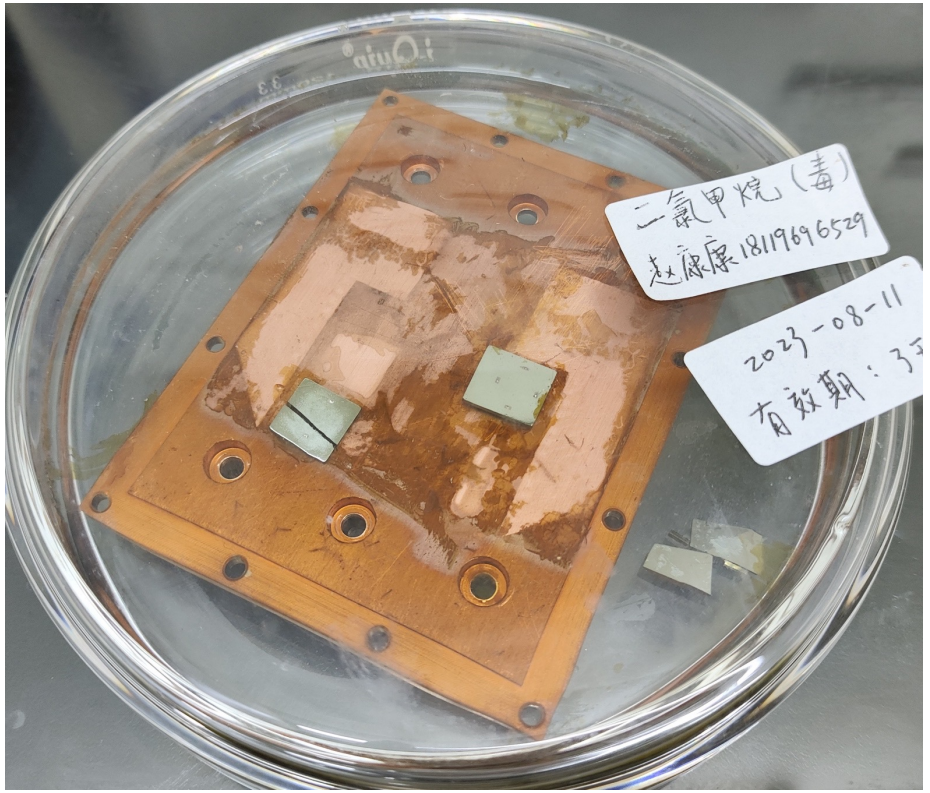


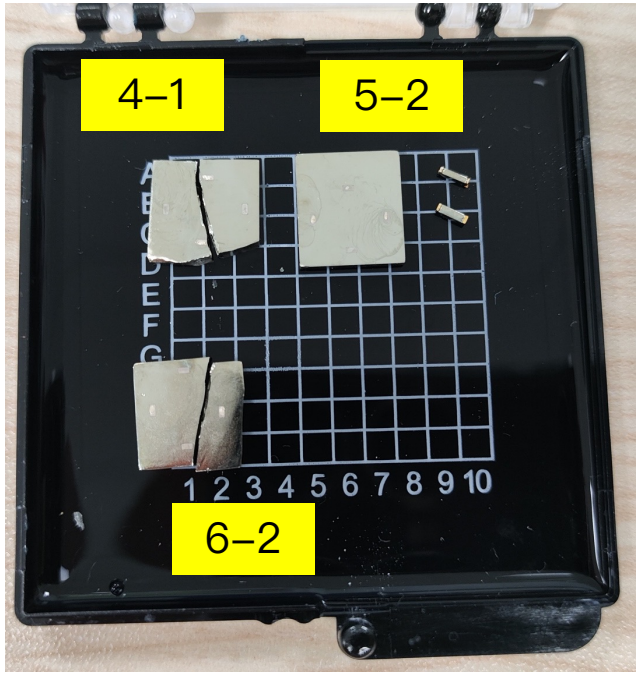
Cr+Al+Cr+Au
50+400+50+ 200

Ungluing

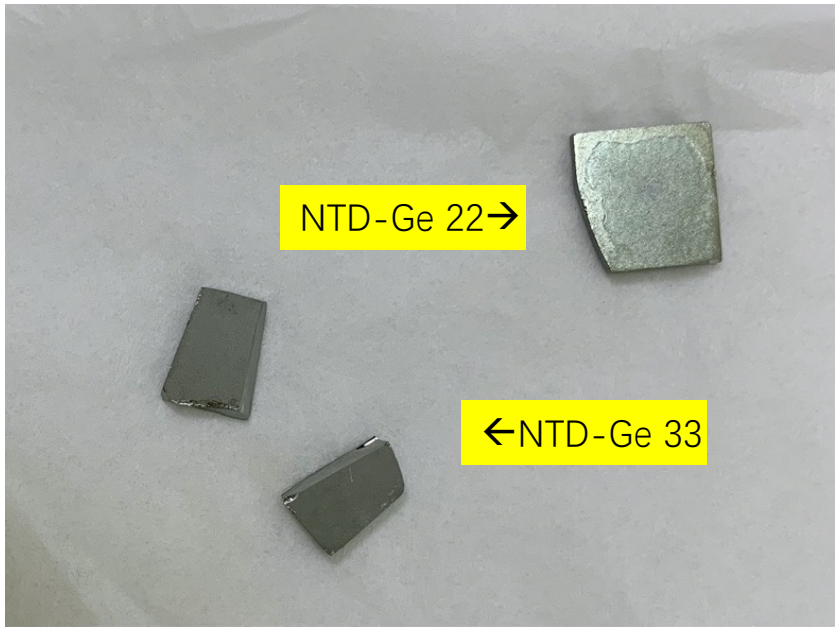
样品碎裂





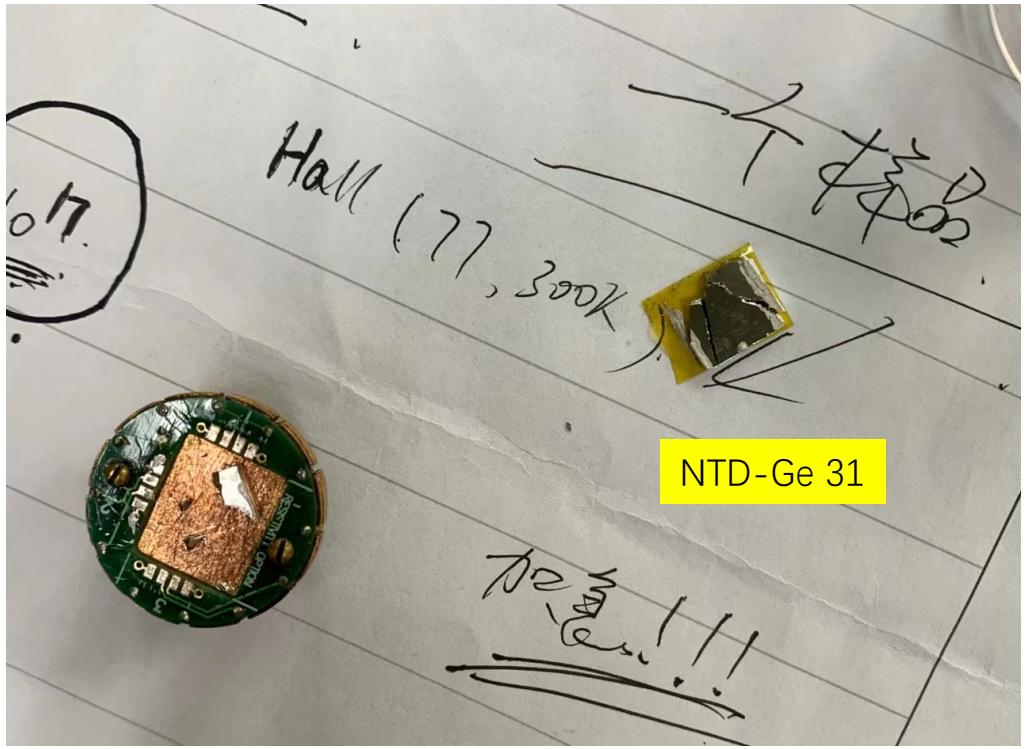


此前碎裂样品



刻蚀，超声清洗时碎裂

猜测为Hall效应测试时，样品翘起，后收到样品杆挤压碎裂



Sample information

碎成两瓣的样品均来自B晶圆

HPGe Number	Pre-treat number	SDD fluence	Hall	PALS	Note	Low T	MS/MOS C-V
7-1	B12	3.17246		✅			❤️
7-3	B21	3.24453				✅	
7-2	A10	3.12200			Jingping		
6-1	B22	5.18569		✅			❤️
6-2	B21	4.91345	✅			❤️	
6-3	A11	4.98445			Jingping		
5-1	B22	5.87180					
5-2	A11	5.95975		✅		❤️	
5-3	A21	5.65041					
1-1	B12	5.72872			Jingping		
1-2	B11	5.35153			Jingping		
1-3	B11	5.61660		✅			
4-1	B22	6.54033		✅		❤️	
4-2	B21	6.27991					
4-3	A11	6.12412			激光		
3-1	B12	7.06805	✅		Broken	❌	❌
3-2	B21	7.63074	✅	✅			
3-3	B21	7.08858	✅		已切割	☑️	
2-1	B22	8.32072	✅	✅	已切割	☑️	
2-2	B12	7.81631	✅				
2-3	B21	❌	❌	❌	Broken	❌	❌

② Process

- Thermal Annealing ✅
- Chemical Etching ❌
- Lapping & Polishing — Dicing ⭕
- Cleaning ⭕
- Mask ⭕
- Ion implantation ⭕
- Etching ⭕
- PVD sputtering ⭕
- Electroplating ⭕
- Post processing ⭕

Lapping & Polishing @ USTC nanoLab*

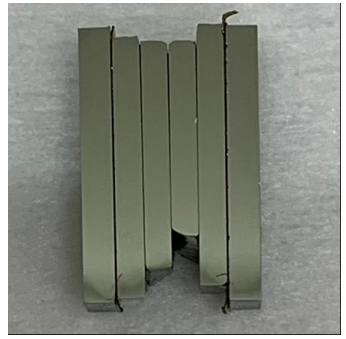
Diamond Lapping Film
SiO2 Suspension

*****苏州纳米虽然抛光效率高，效果好，但是代加工程序复杂*


METPREP 3
PH-3
ALLIED
HIGH TECH PRODUCTS, INC.
AD-5
1 2 3 4 5
DISPENSER POSITION
STOP
START
ALLIED
HIGH TECH PRODUCTS, INC.

② Process

- Thermal Annealing ✅
- Chemical Etching ❌
- Lapping & Polishing — Dicing ⭕
- Cleaning ⭕
- Mask ⭕
- Ion implantation ⭕
- Etching ⭕
- PVD sputtering ⭕
- Electroplating ⭕
- Post processing ⭕



Lapping & Polishing @ USTC nanoLab*

日化精工固体蜡
60度可溶，可酒精清洗
粘接力强

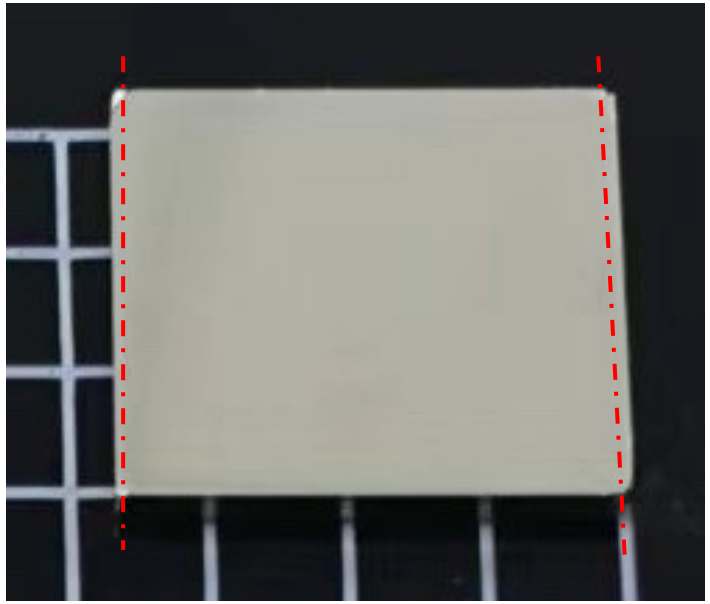
■ 物理特性

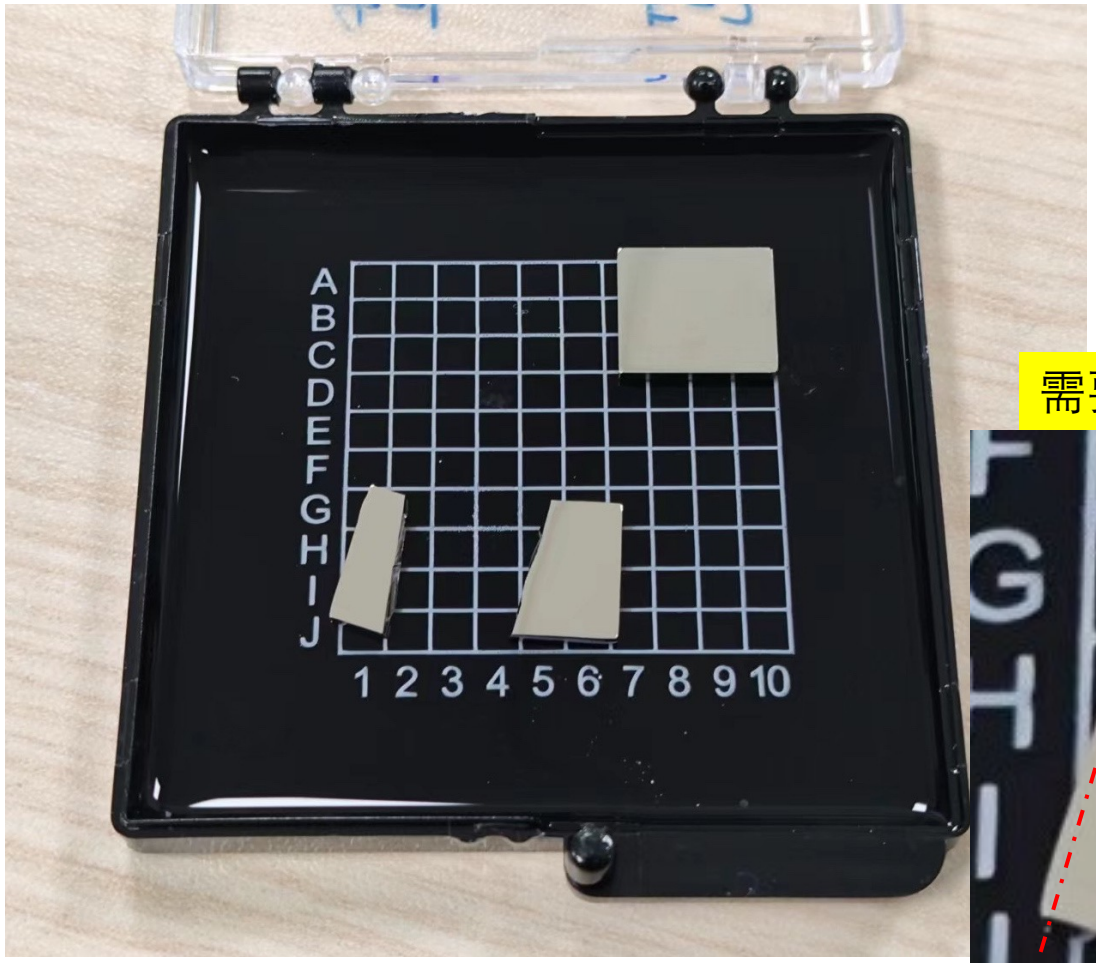
项目	单位	艾鲁克瓦克斯 5302	艾鲁克瓦克斯 542SL	艾鲁克瓦克斯 5402SL	艾鲁克瓦克斯 552
软化点	℃	58	55	53	52
接着力	N/mm2	2.4	3.4	3.0	4.4
	kgf/cm2	24	35	31	45
流动粘度	cP・60℃	160	-----	120	-----
	cP・80℃	40	990	46	1,100
	cP・100℃	27	230	45	220
	cP・120℃	-----	80	-----	70
针入度	200g/60sec.	6	6	10	3
比重	at 25℃	0.98	1.00	0.97	1.00
推荐涂布温度※1	工件表面温度（℃）	70 - 100	90 - 100	60 - 150	80 - 120

**苏州纳米虽然抛光效率高，效果好，但是代加工程序复杂*

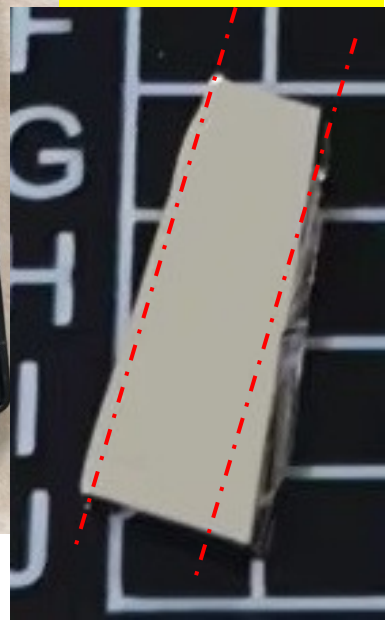
Polishing and Dicing

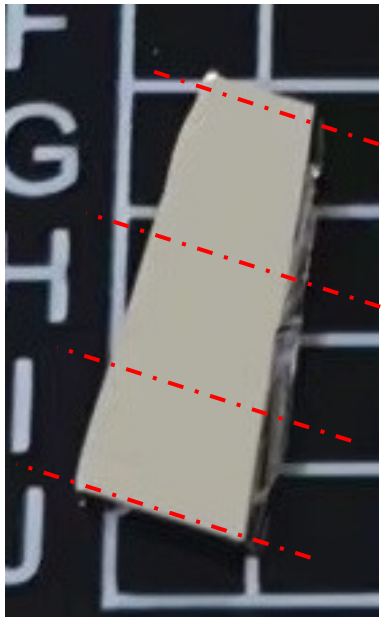
大样品包裹型电极制作难度较大

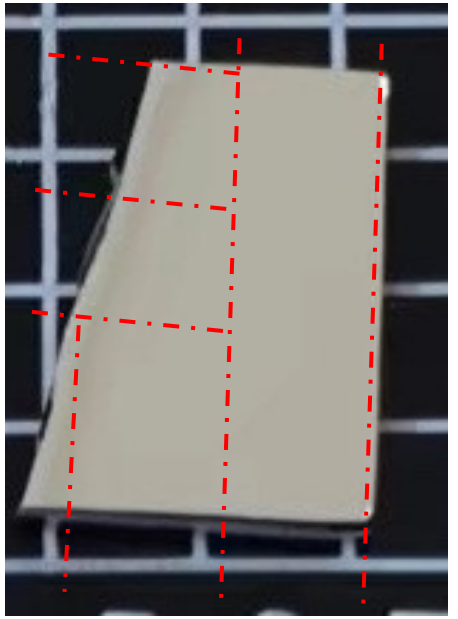




需要>3.1 mm







Dicing

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7-3	1.27	11.72
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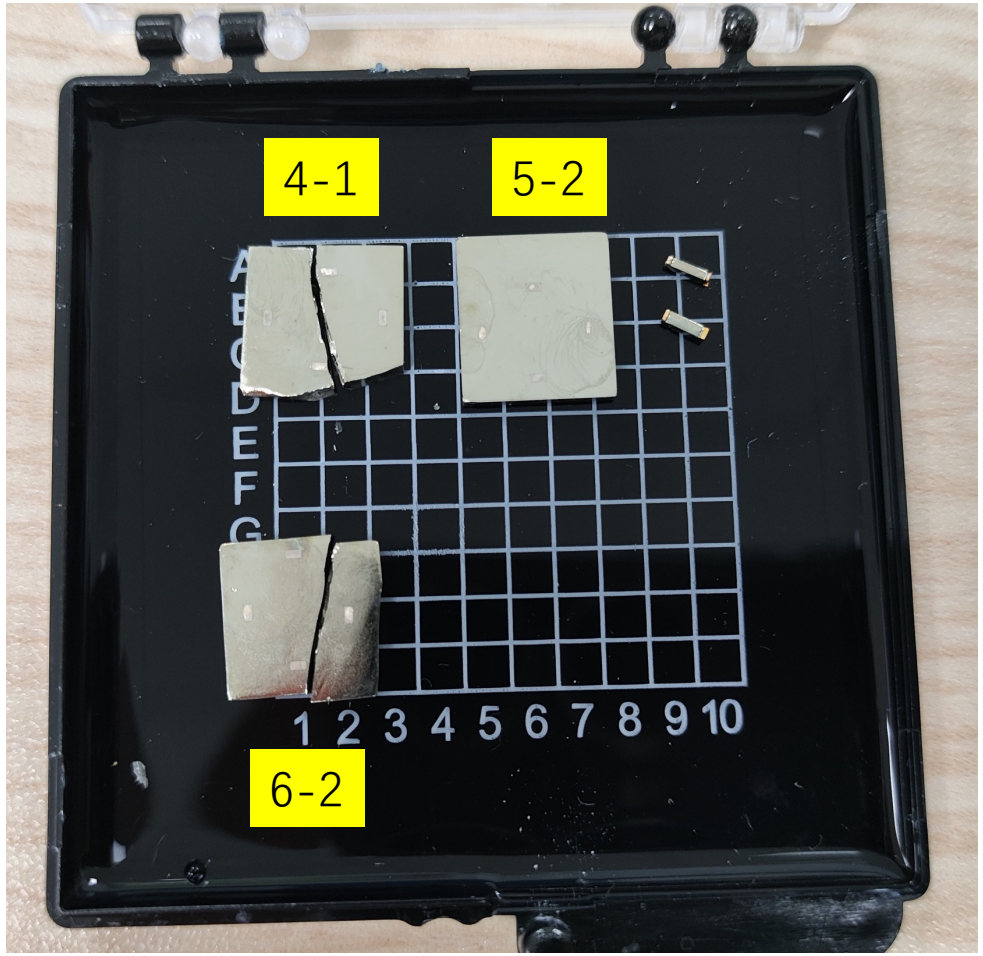
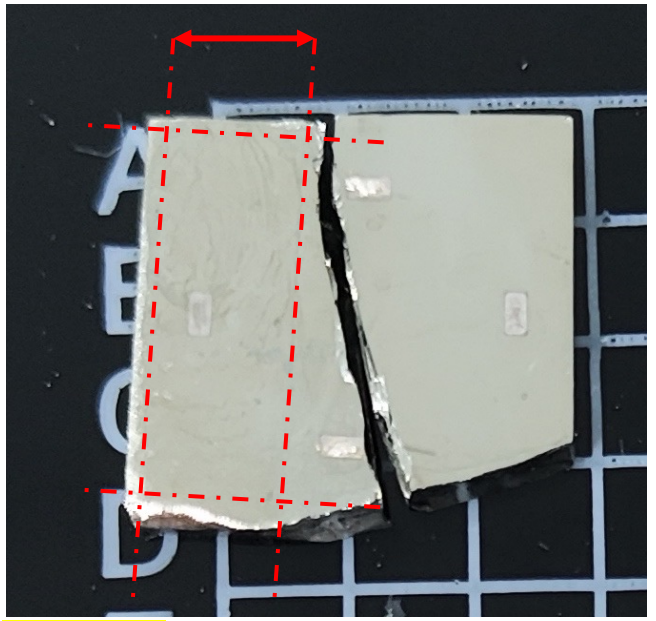
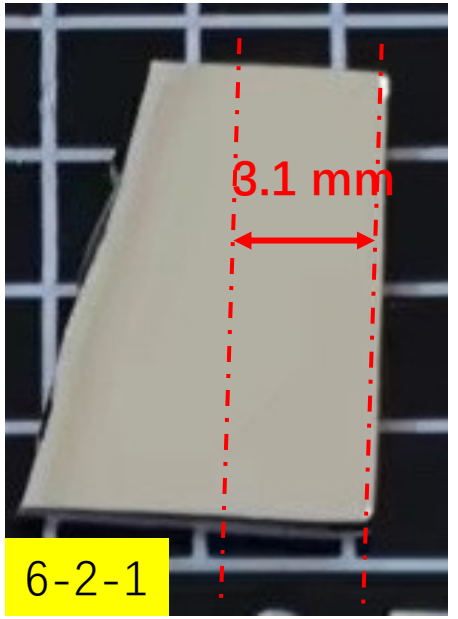


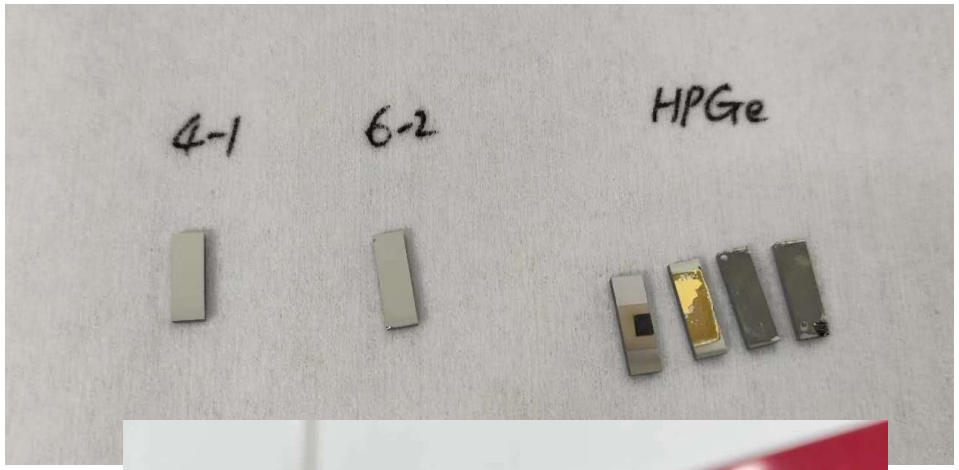


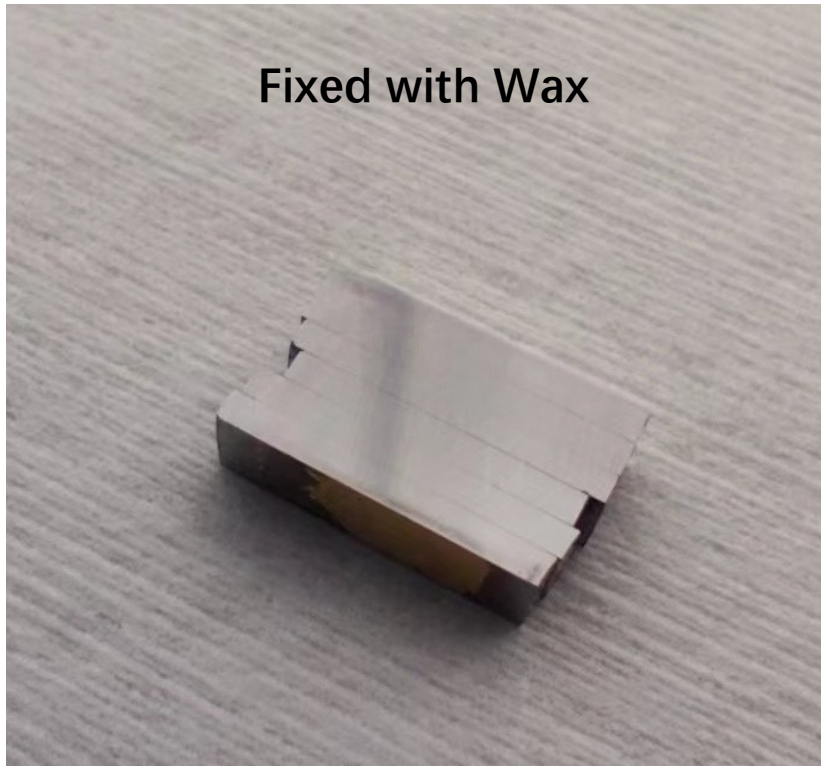
4-1-1



6-2-1

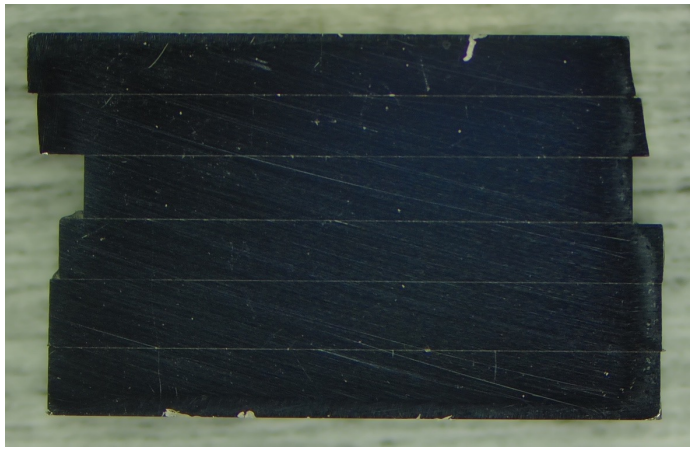
Side polish

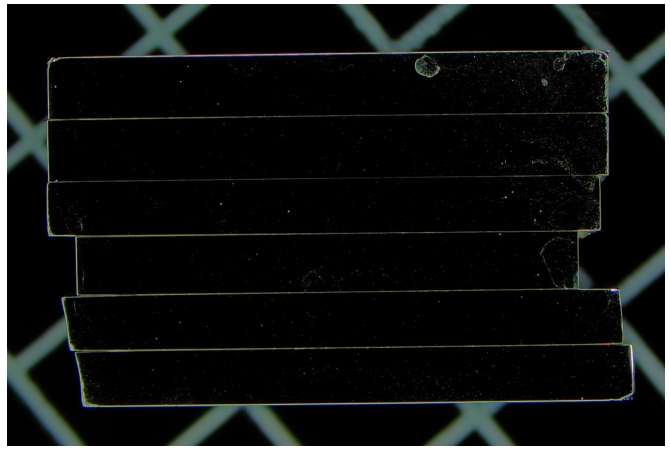


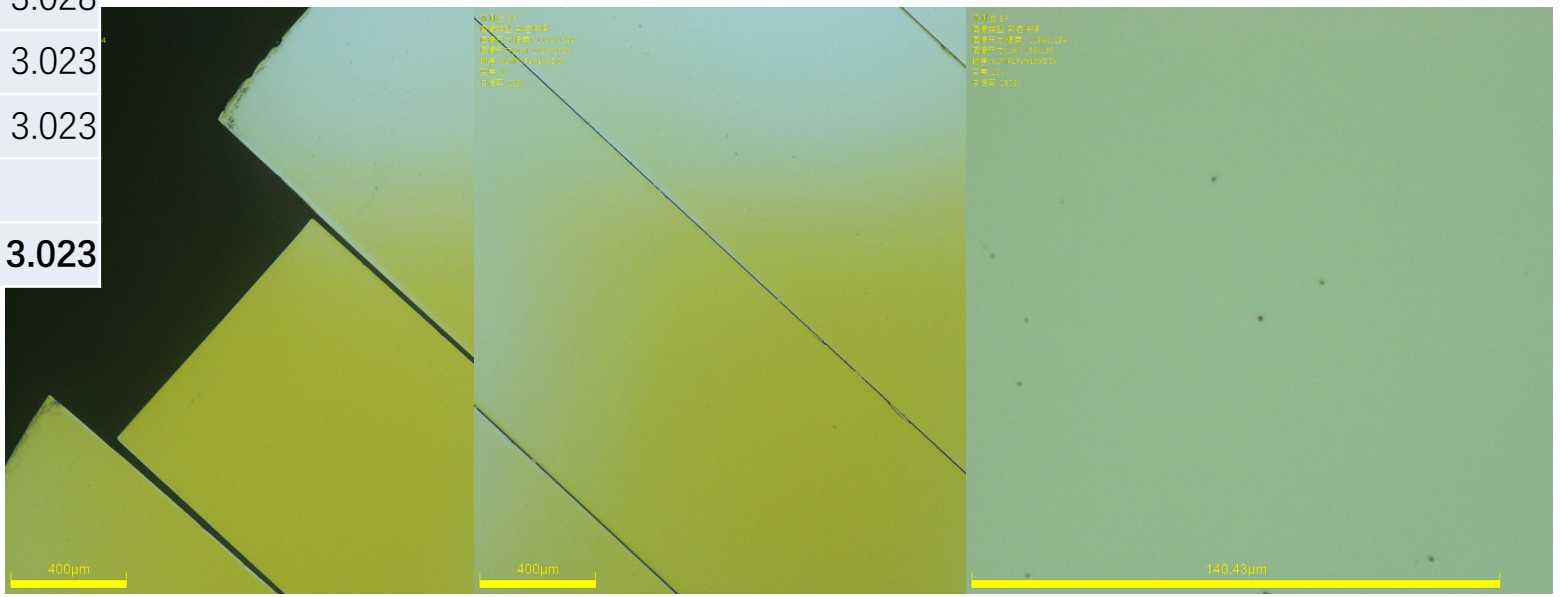


Thickness reduction when Lapping

Lapping Film	NTD-Ge side
before	3.121
9 um	3.062
6 um	3.035
3 um	3.028
1 um	3.023
0.5 um	3.023
~~0.25 um~~	
final (SiO2+H2O)	**3.023**





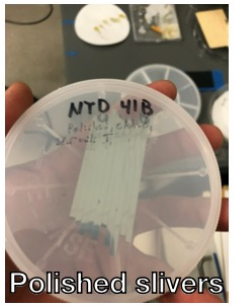


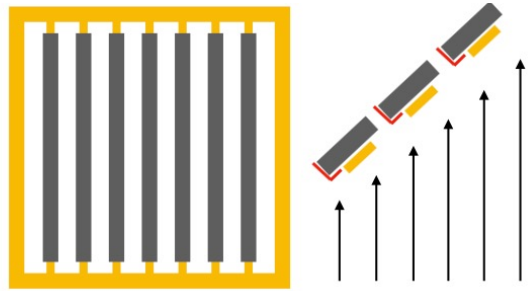
Next: AFM measurement

② Process

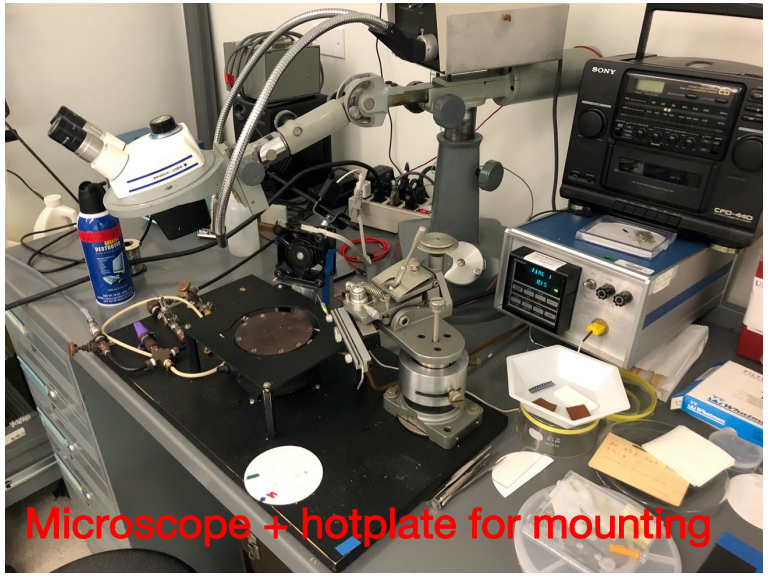
- Thermal Annealing
- Chemical Etching
- Lapping & Polishing
- Dicing
- Cleaning
- Mask
- Ion implantation
- Etching
- PVD sputtering
- Electroplating
- Post processing

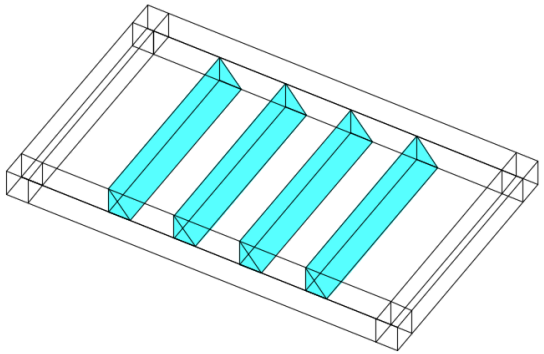
Mask:





Using Wax





Epoxy

Gluing station

弹簧吸杆

Signal simulation

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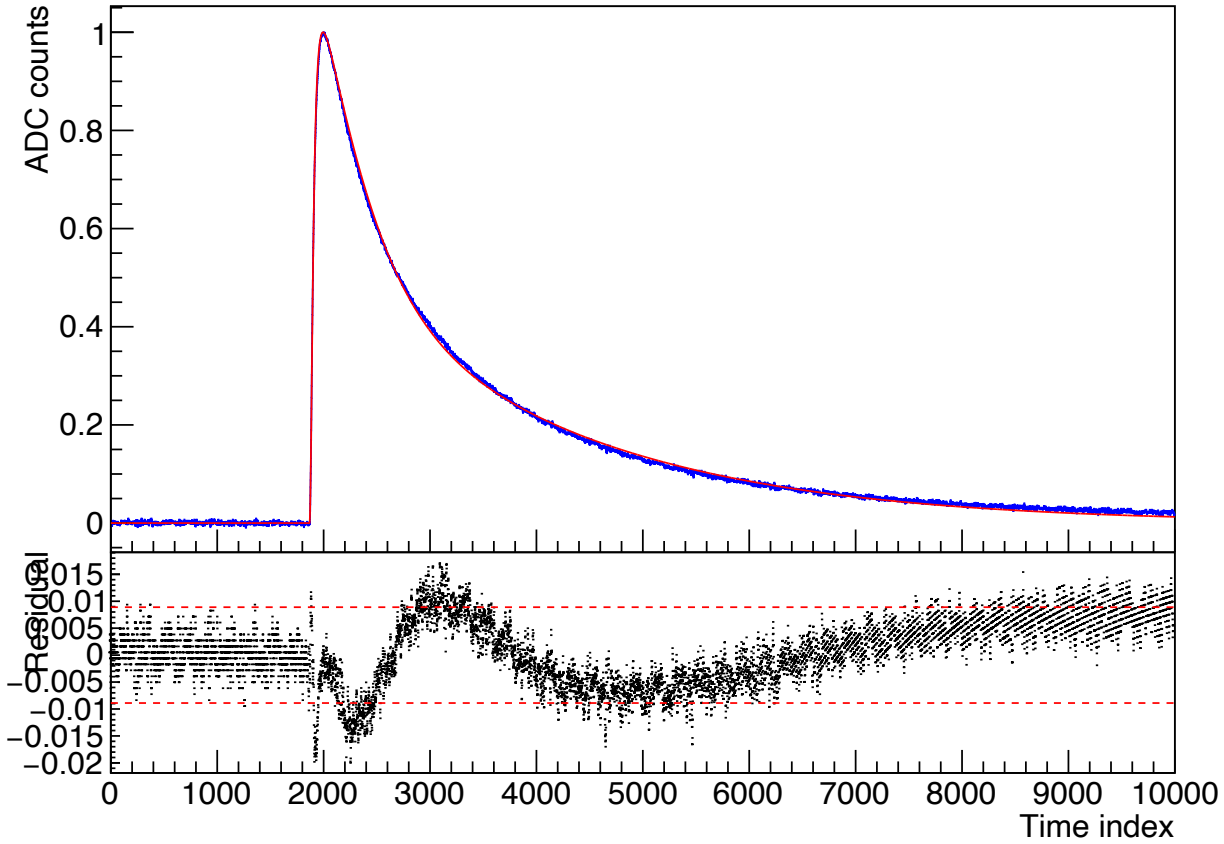

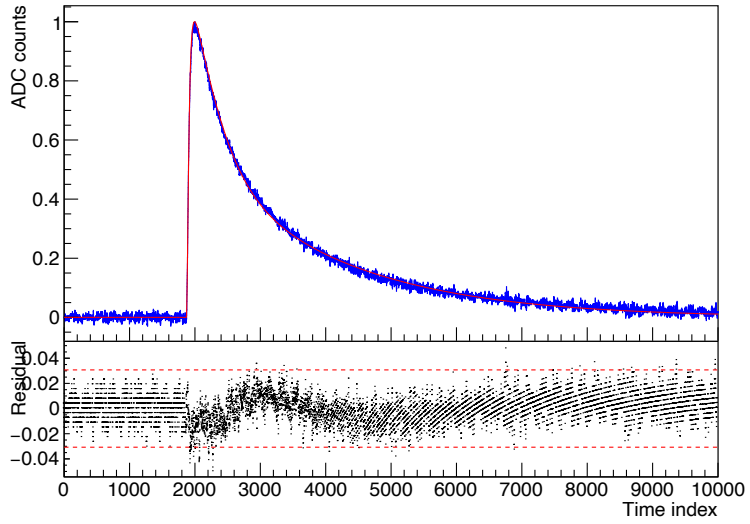

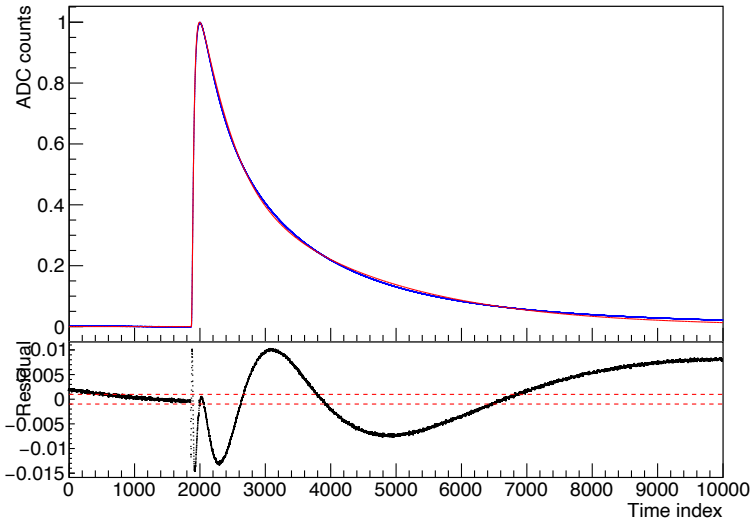

Noise simulation

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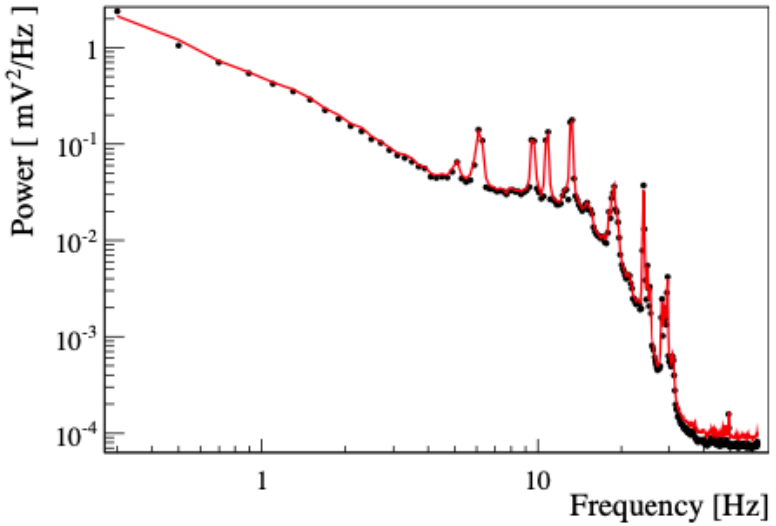
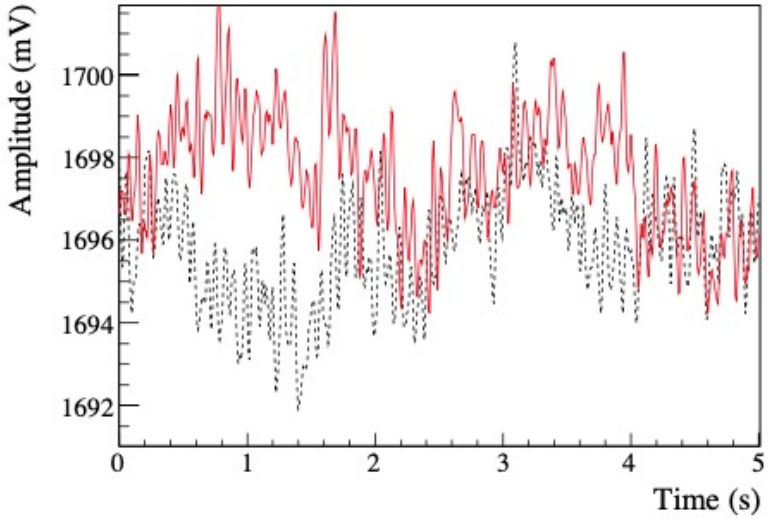
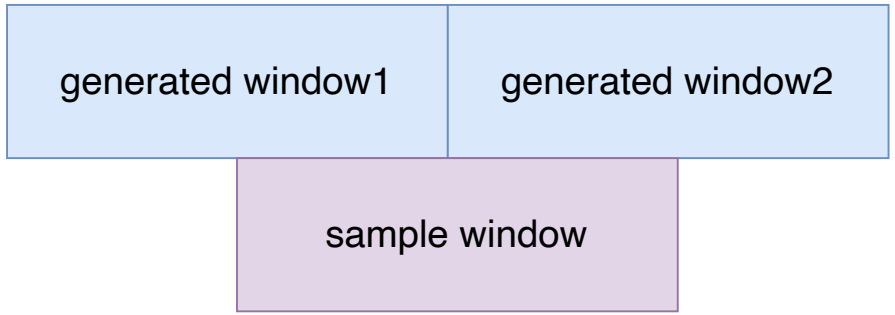




- Given the desired noise power spectrum $N(\omega)$ select the basis function $f(t)$ according to Eqs. (4) and (5). Then Eq. (2) fixes the constant α.
- Generate a set of increasing delays t_k according to the Poisson distribution with average rate λ.
- Generate the random amplitudes a_k according to an arbitrary distribution with variance fixed by Eq. (10).
- Shift $f(t)$ by t_k imposing a periodicity constraint $f(t) = f(t+T)$ and multiply the result by a_k.
- Sum iteratively over t_k while $\sum t_k < T$.

How to?

Time series with a fixed length → Continuous noise



不连续

Equal average NPS?

Noise generation

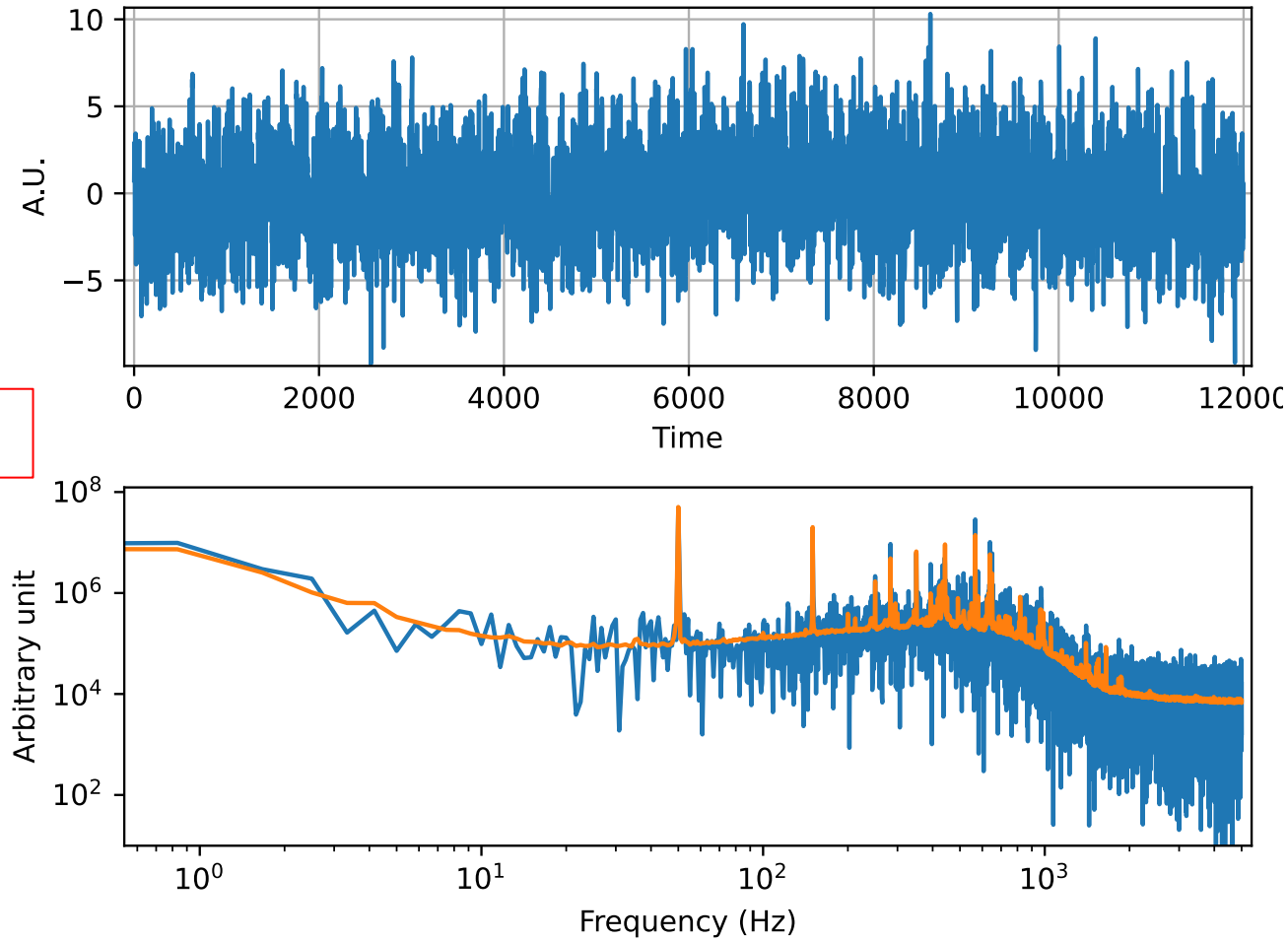
$$n(t) = \sum_k a_k f(t - t_k)$$

$$F[k] \equiv \sqrt{N[k]} \cdot e^{i\theta_k}$$
$$f[k] = \mathcal{F}^{-1}\left(F[k]\right)$$

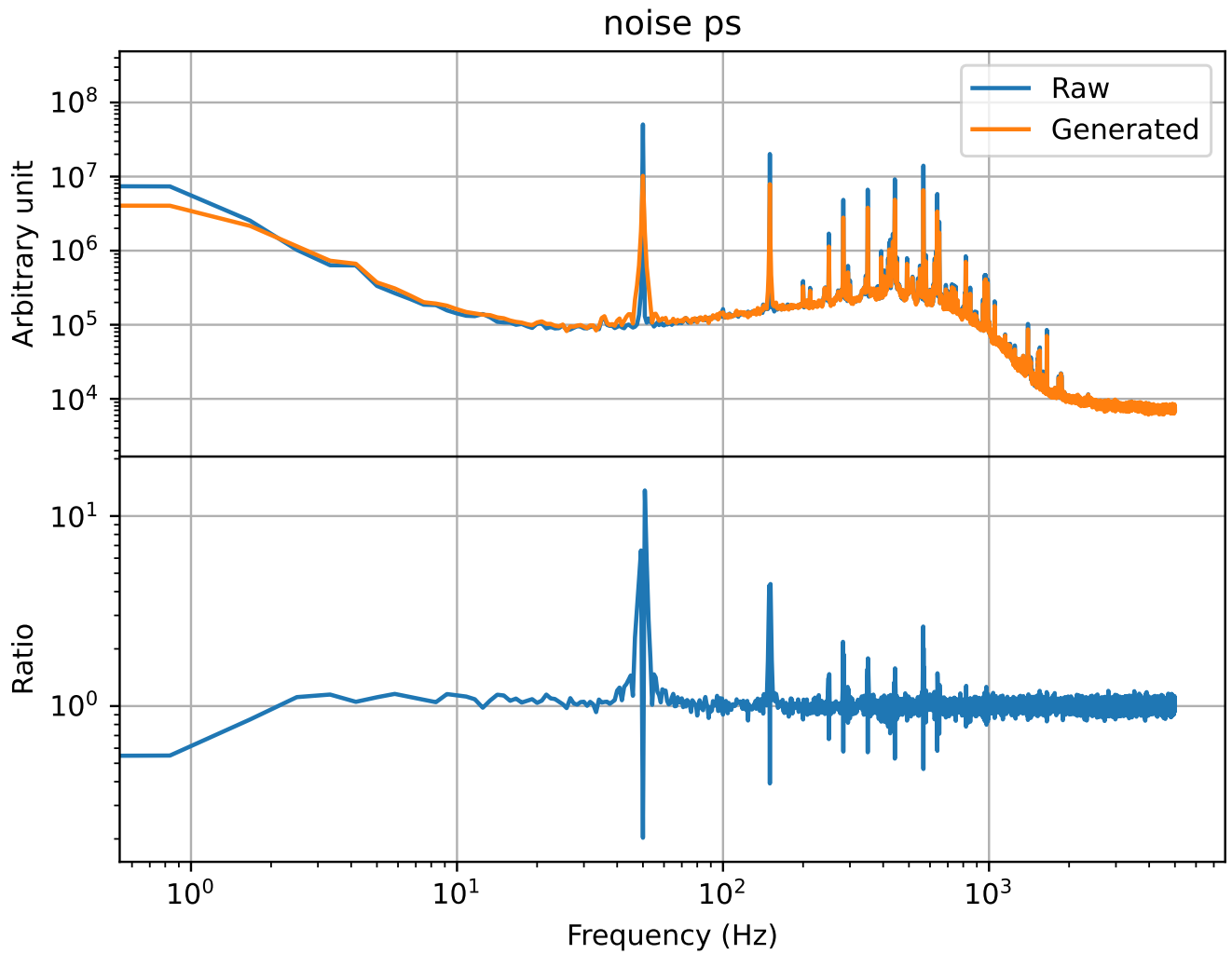
$$t_k = t_{k-1} - \ln(1 - R)/\lambda$$

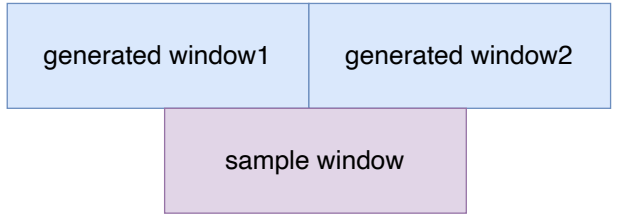
$$N(\omega) = \left\langle \left| \mathcal{F}\left[\sum_k a_k f(t - t_k) \right] \right|^2 \right\rangle$$
$$= \left\langle \left| F(\omega) \right|^2 \cdot \sum_{ij} a_i a_j e^{i\omega(t_j - t_i)} \right\rangle$$

$$N(\omega) = \left\langle \left| F(\omega) \right|^2 \right\rangle \left\langle \sum_{k=1}^{L} |a_k|^2 \right\rangle$$



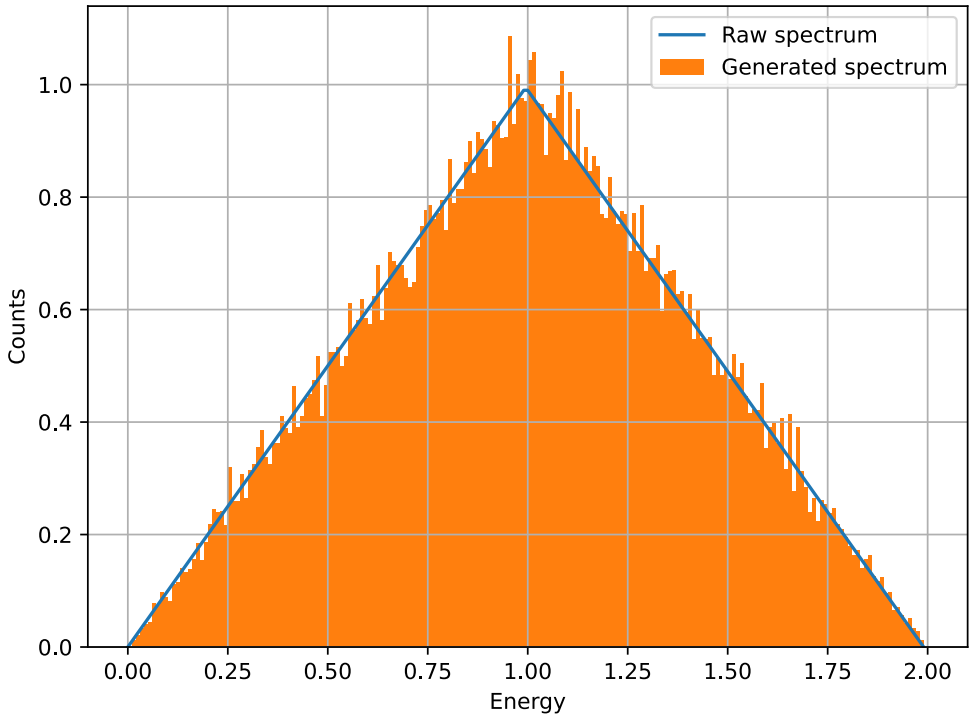
Generated noise: power spectrum

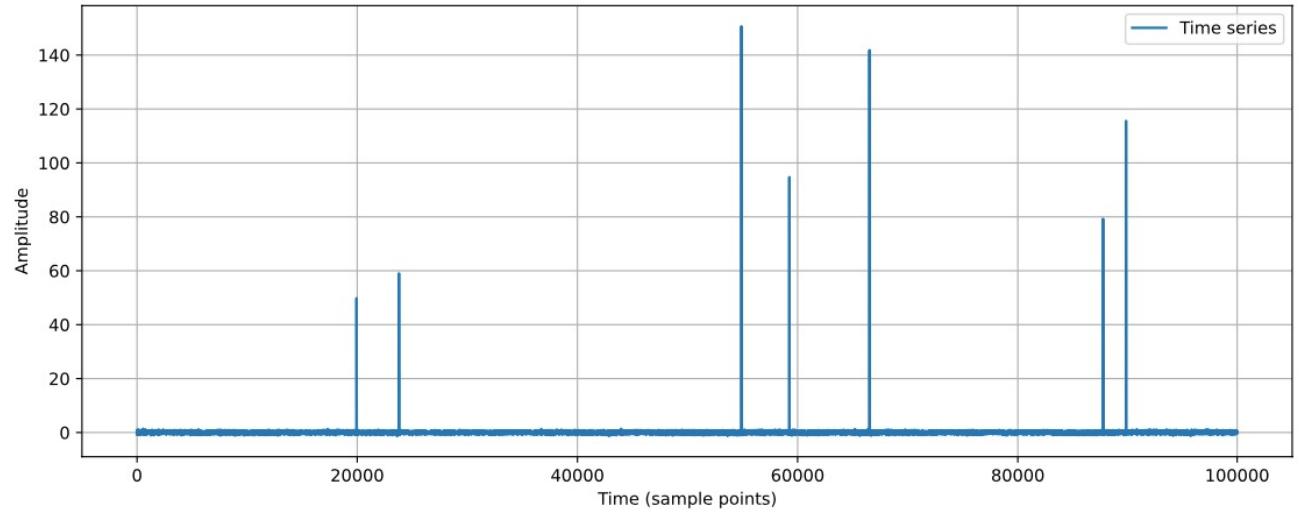


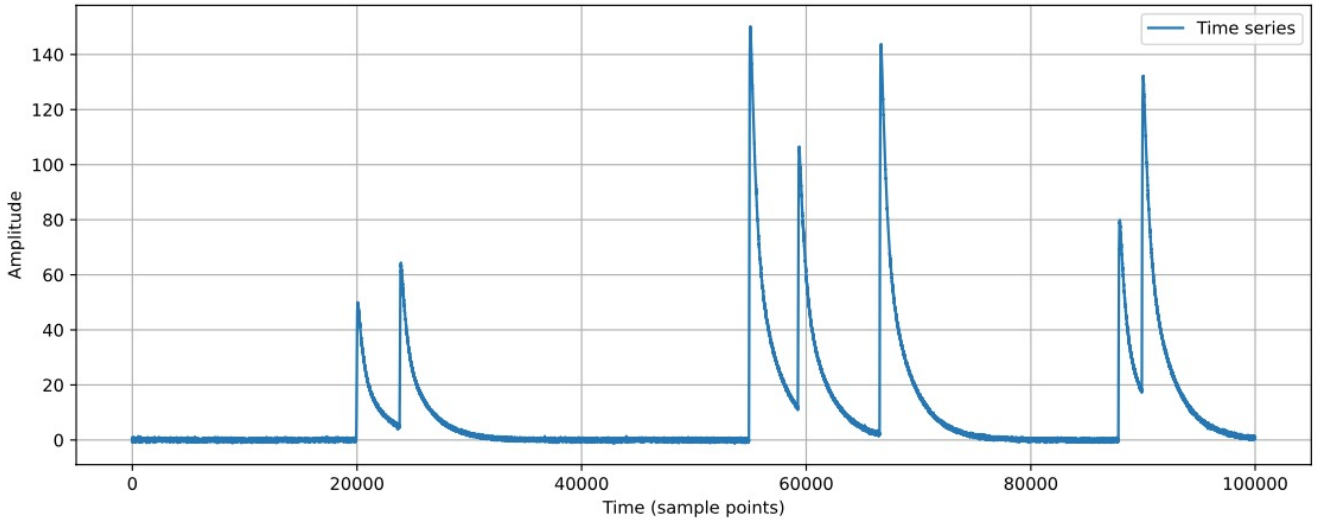


Equal average NPS?

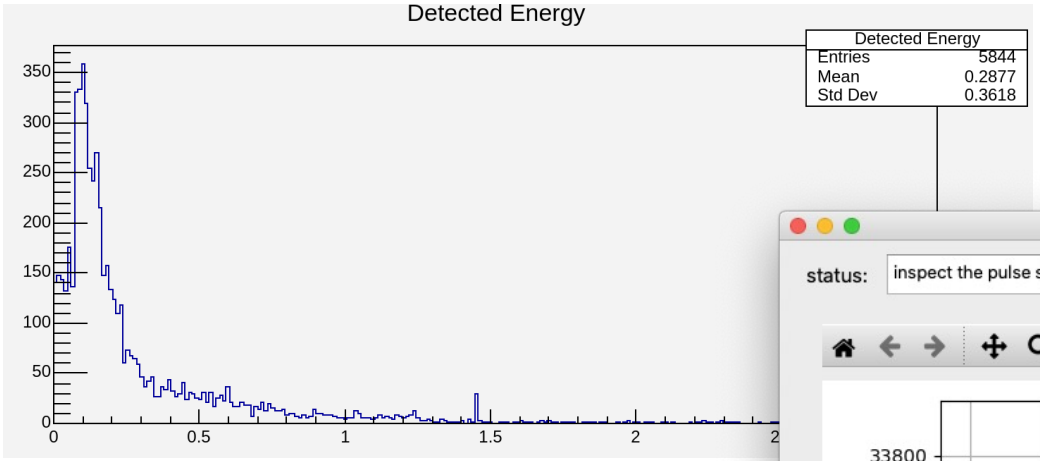
Signal generation

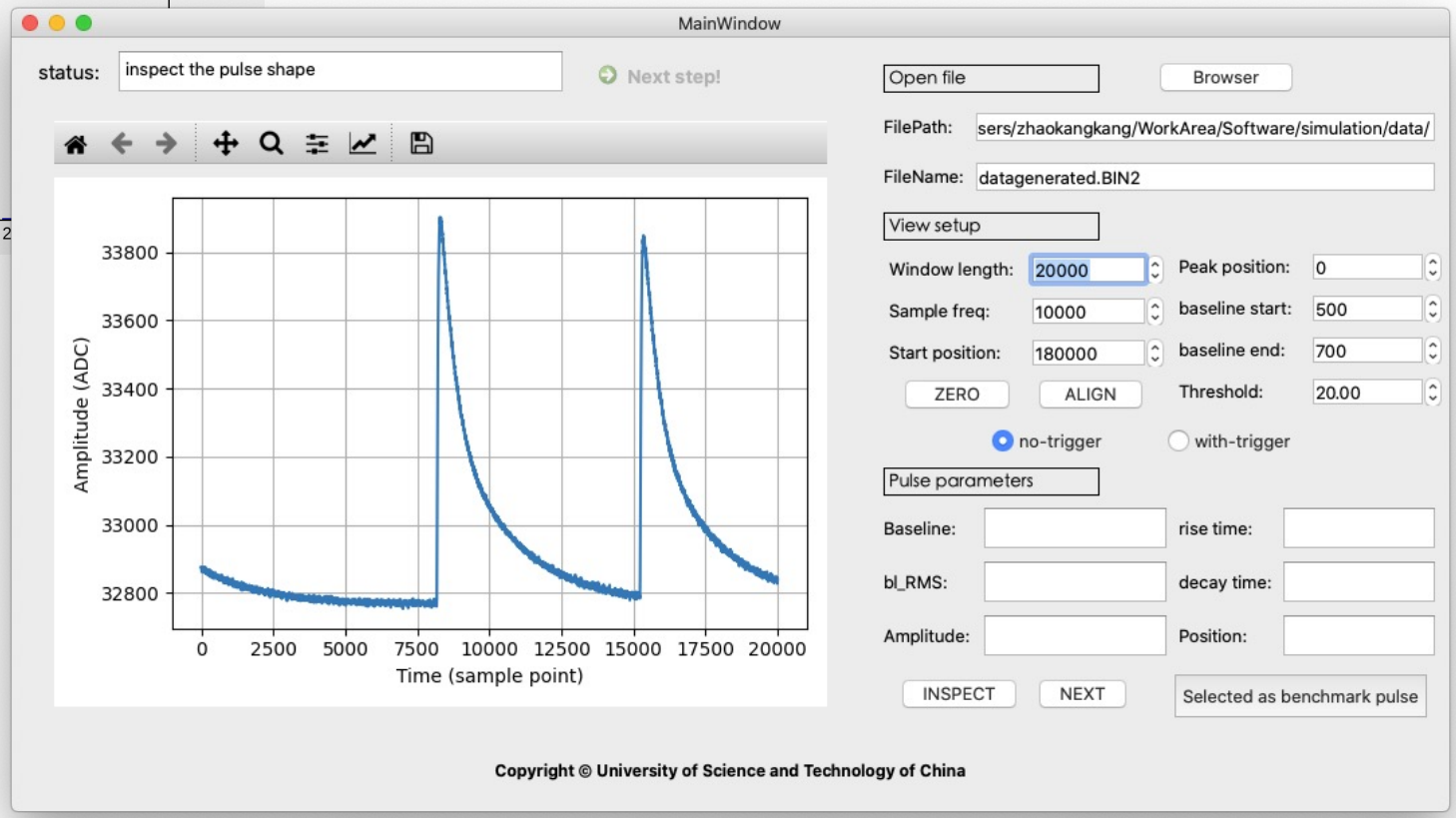






Pretreatment program





Etching: 干法刻蚀

after ion implantation

before PVD sputtering

② Process

- Thermal Annealing
- Chemical Etching
- Lapping & Polishing — Dicing
- Cleaning
- Mask
- Ion implantation
- Etching
- PVD sputtering
- Electroplating
- Post processing

需进一步调研：参考NTD电极厚度，电镀工艺

Electroplating:

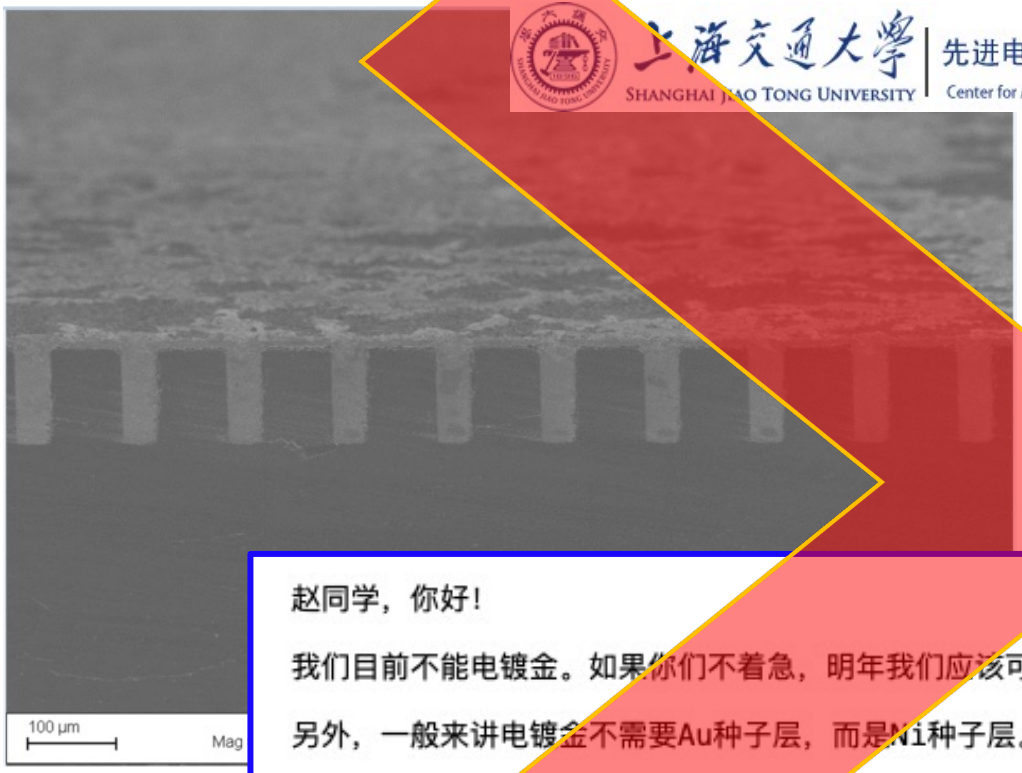
after PVD sputtering, make thick Au metal layer > 1 um

1. stem layer AZ9562
2. Au seed layer 100nm
3. absorber layer AZ 125nXT 100um thick
4. gold electroplating 100um
5. resist removal DMF solvent or DMSO

all chemicals can be found at microchemicals including gold plating solution.

电镀可以形成均匀、致密、结合力良好的金属层，与CVD、PVD等薄膜沉积技术相比较，精确复制某些复杂或特殊形状的器件，并且可以无限增加金属厚度。

Electroplating



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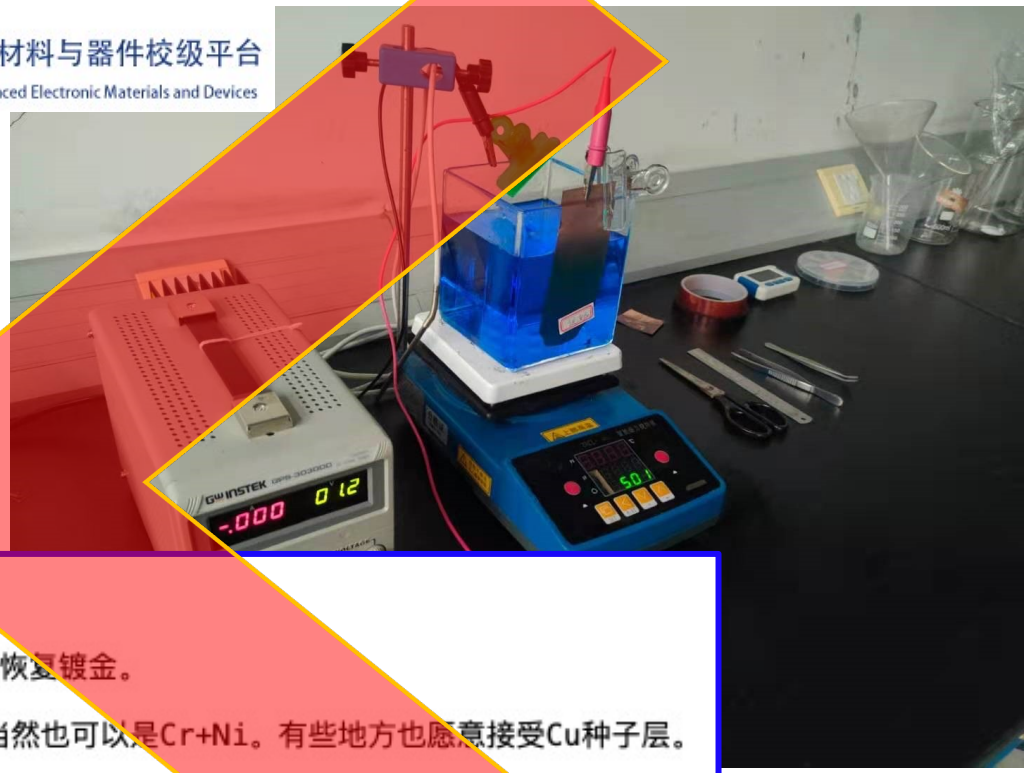
先进电子材料与器件校级平台
Center for Advanced Electronic Materials and Devices



赵同学，你好！

我们目前不能电镀金。如果你们不着急，明年我们应该可以恢复镀金。

另外，一般来讲电镀金不需要Au种子层，而是Ni种子层。当然也可以是Cr+Ni。有些地方也愿意接受Cu种子层。

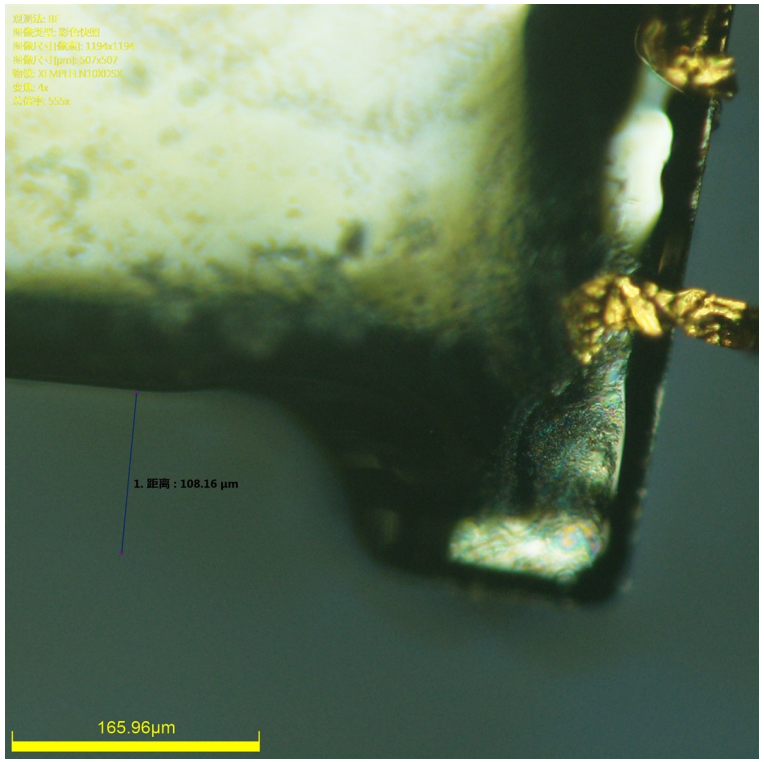
3mm的样品面积太小了，很难得到均匀电场，因为一般电镀液阳极面积都比较大的。

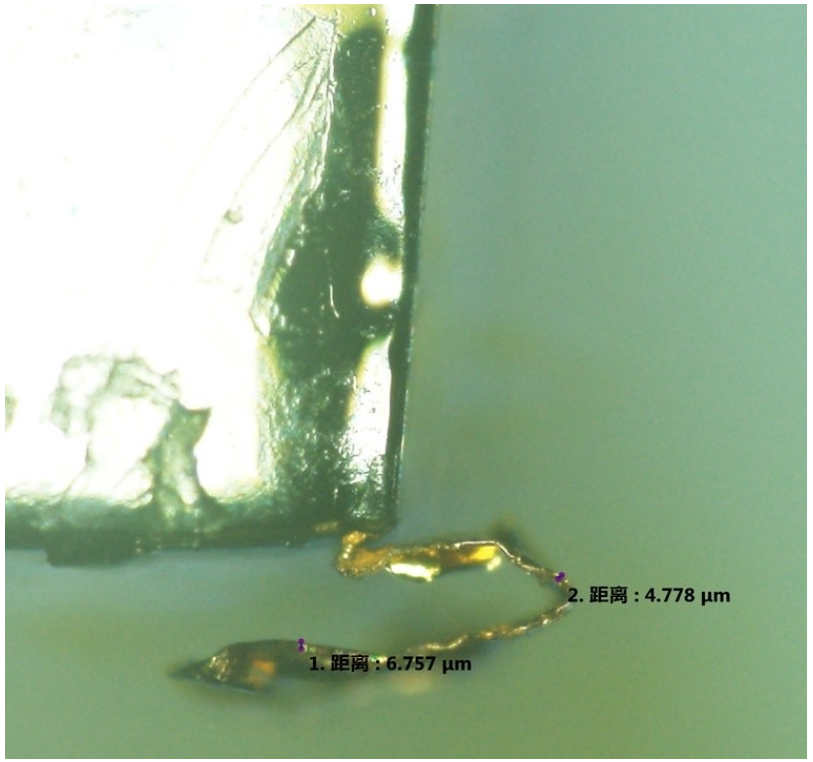
希望有帮到你，

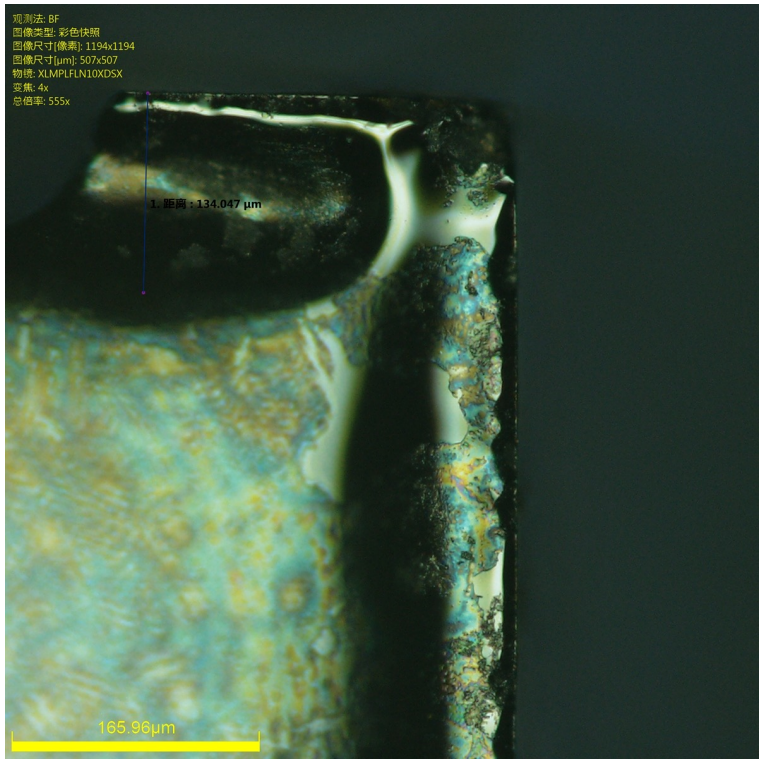
田苗

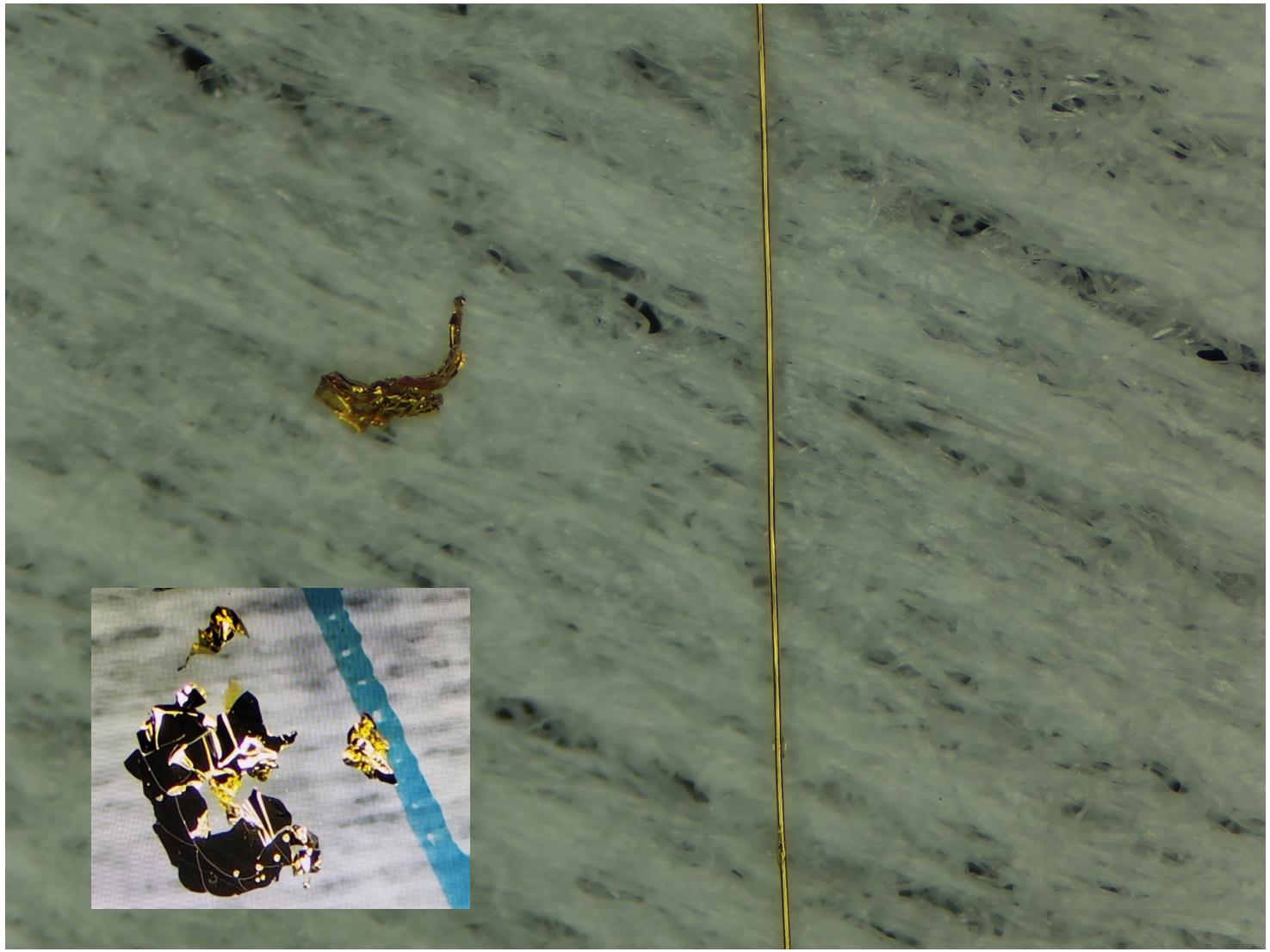
REF light NTD

刻蚀深度大于100 μm









② Process

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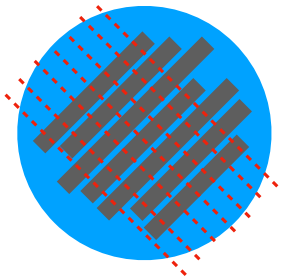
Post processing：

Thermal Annealing and chemical etching

The CUORE NTD Process: Dicing

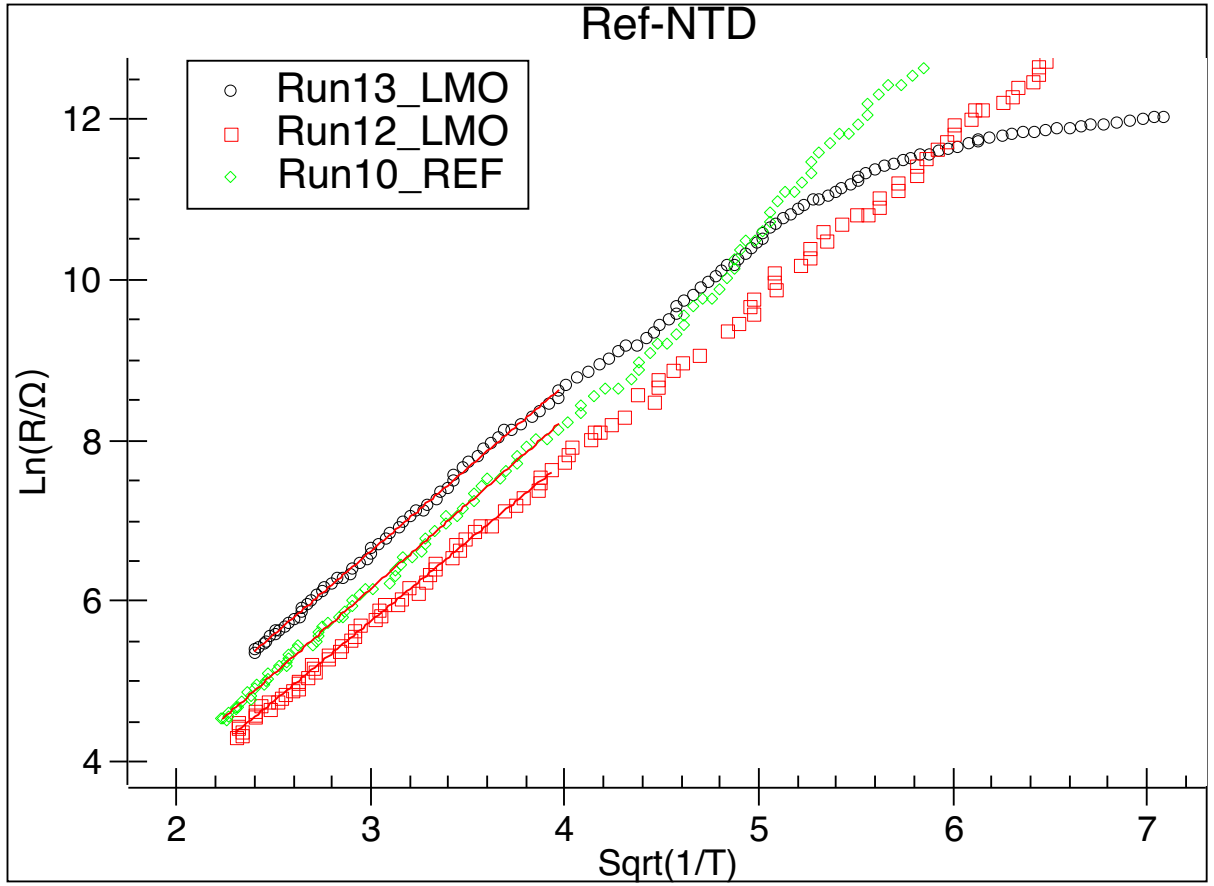
1. Mount slivers on sacrificial Si wafer with wax
2. Cross-cut: *this sets the length of the chips (between non-contact sides).*
   A. Target = 2.900 mm; Factoring in etch → cut 2.925 mm
3. Stream etch in saw cuts, 12 sec. 7:2:1
4. Dismount from wafer/wax
5. Final etch all surfaces 30 sec. 7:2:1.
6. Done!

Estimate: 1 day



6

LMO-NTD 测量



Run10: Installed at cooper
Run12: couple to LMO
Run13: couple to LMO

5T6. i.e. LMO-NTD.		
Run10.	0.083 ± 0.03 Ω	4.47 ± 0.05 K
Run12	0.081 ± 0.04 Ω	3.96 ± 0.06 K
Run13	1.50 ± 0.05 Ω	4.29 ± 0.05 K