用于CEPC内层顶点探测器的高计数率CMOS像素探测器芯片研制

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On behalf of the CEPC MOST2 Vertex detector design team

第三届半导体辐射探测器研讨会

5月11-14日，2023

内容概要

- 项目背景
- TaichuPix 芯片概述
- TaichuPix 芯片设计与测试
- 总结与展望

CEPC 顶点探测器需求

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

➔ Impact parameter resolution,

$$\sigma_{r\phi} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)}\ (\mu m)$$

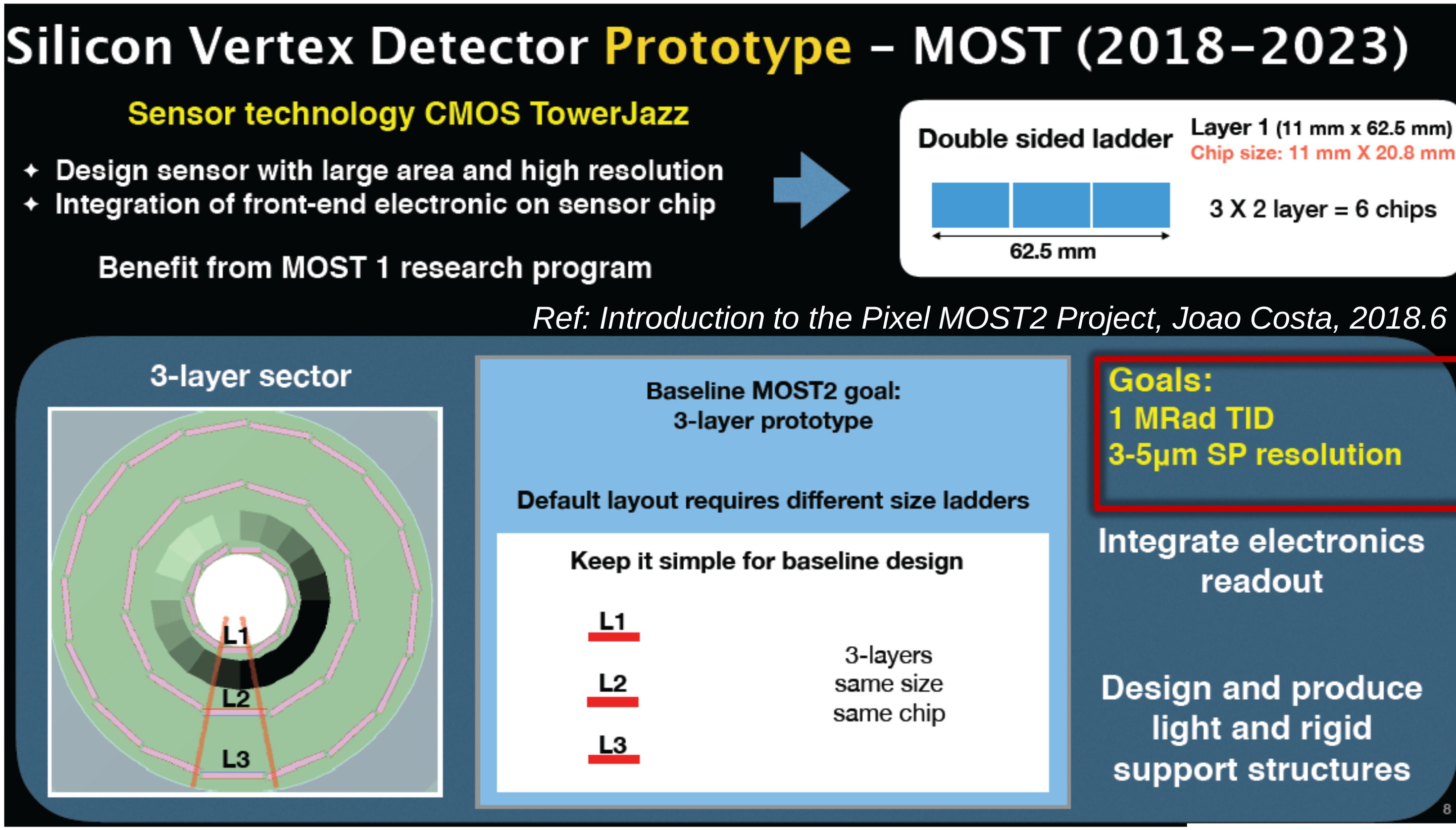
Physics driven requirements		**Running constraints**		**Sensor specifications**	
$\sigma_{s.p.}$	2.8 μm			Small pixel	~16 μm
Material budget	0.15% X_0/layer			Thinning to	50 μm
		Air cooling		low power	50 mW/cm²
r of Inner most layer	16 mm	beam-related background		fast readout	~1 μs
		radiation damage		radiation tolerance	≤3.4 Mrad/ year ≤6.2×10¹² n_{eq}/ (cm² year)

Baseline design parameters for CEPC vertex detector

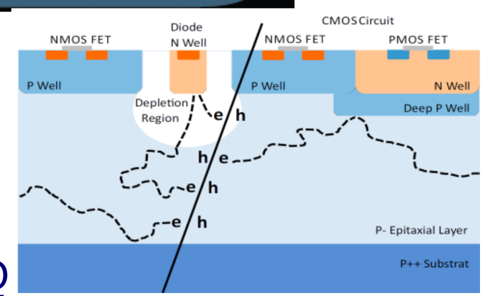
	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ(μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

TaichuPix 芯片研发背景



- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ

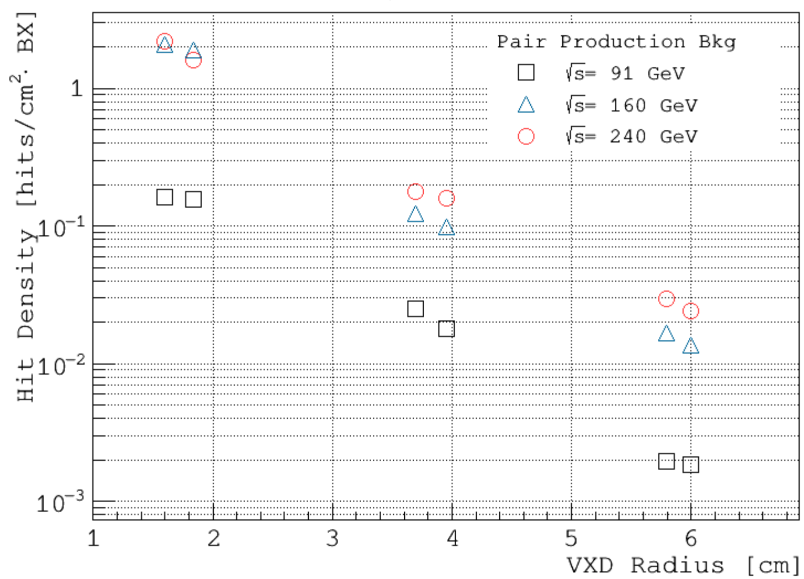


CMOS pixel sensor

TaichuPix 芯片设计指标

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm

Hit Density vs. VXD Radius

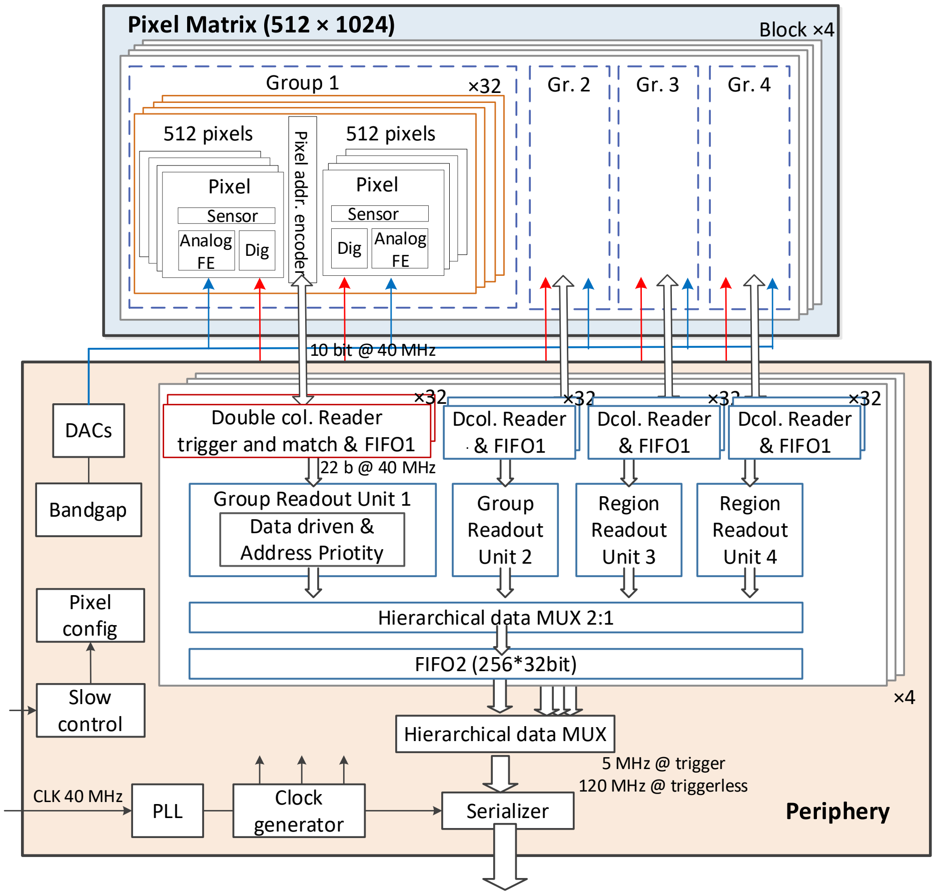


Ref: CEPC Conceptual Design Report, Volume II

For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns (for 98% efficiency)	Chip size	~1.4 cm × 2.56 cm

TaichuPix 芯片结构

Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype

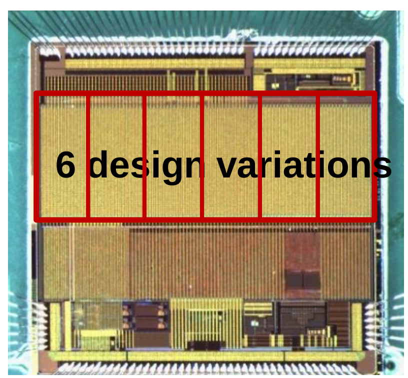


- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - **Time stamp added at EOC**
  - **Readout time**: **50 ns** for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

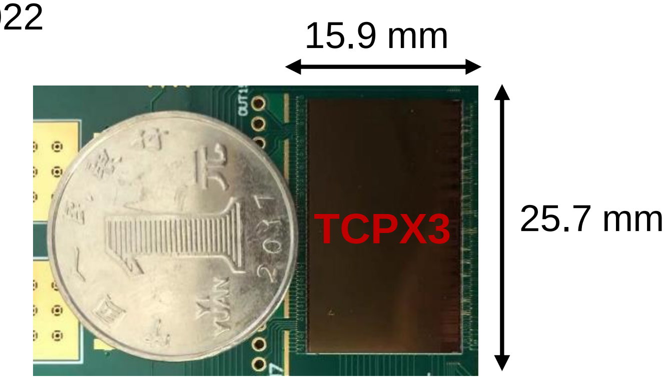
TaichuPix 原型芯片概述

- **Major challenges for the CMOS sensor**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 round of sensor prototyping in 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019.06 – 2019.11
    - TaichuPix-2: 2020.02 – 2020.06
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022

TaichuPix-1



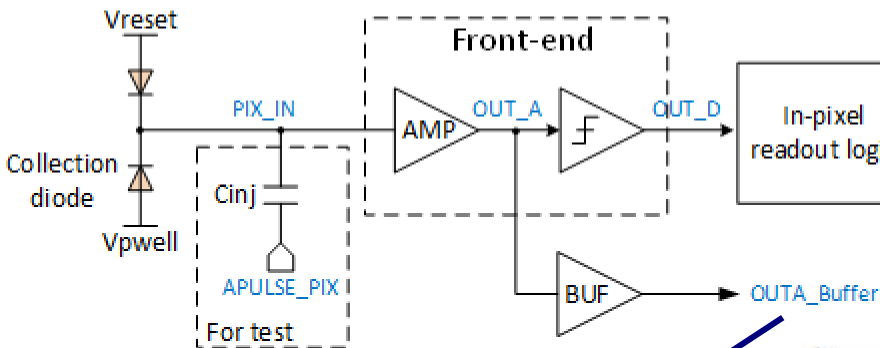
TaichuPix-2

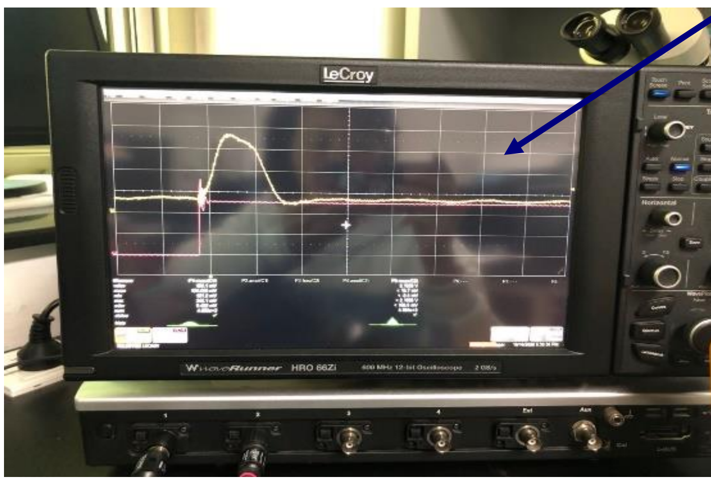


TaichuPix-3
Pixel size：25 μm × 25 μm

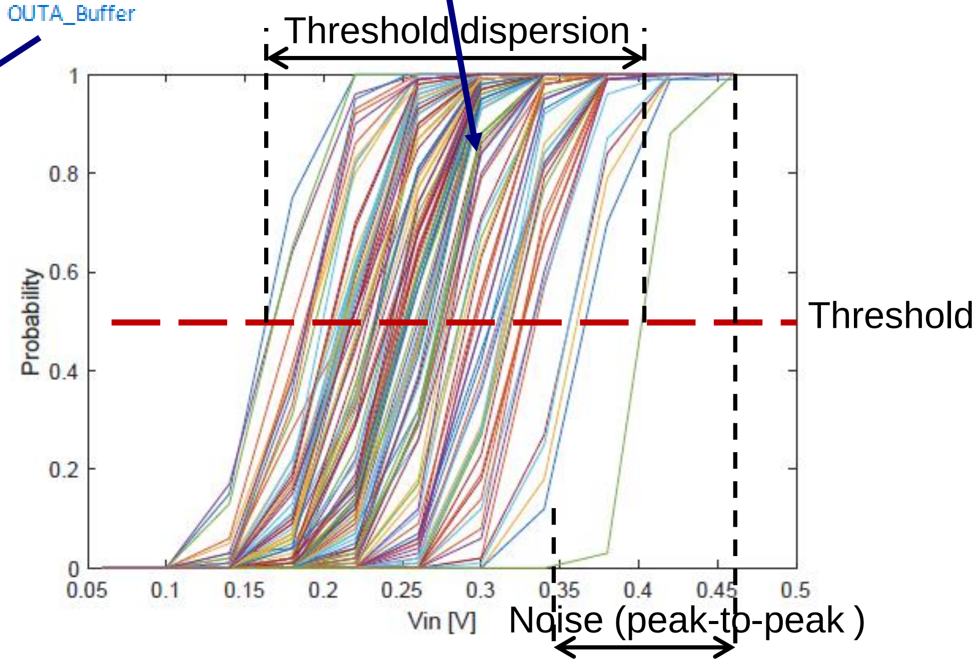
Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**





Analog output of a pixel @ Vin = 0.9 V

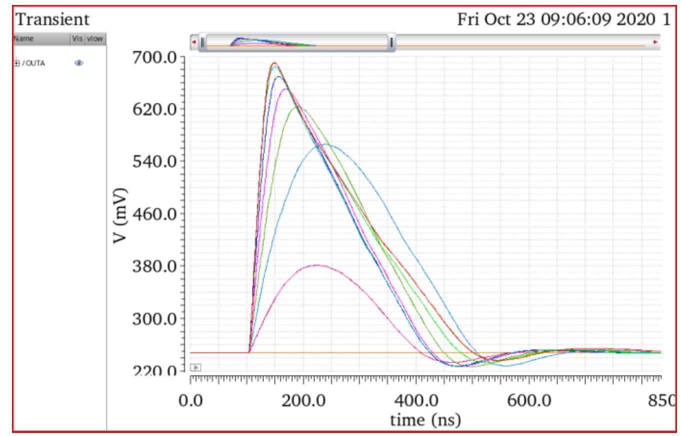


Measured “S-curve” for 128 pixels

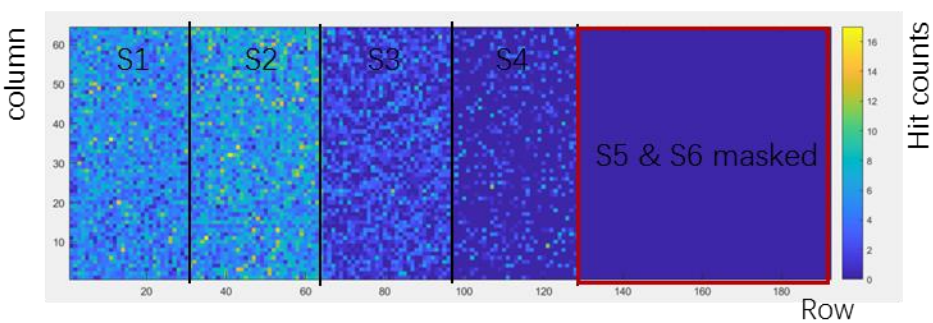
Functionality of complete signal chain of TaichuPix2

- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with an X-ray source and a laser source.**

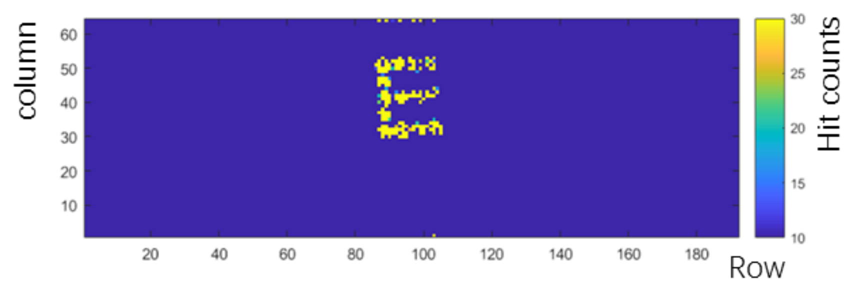
TaichuPix2 response to **X-ray** tube (cutting energy @ 6keV)



Simulated analog output with different input signal



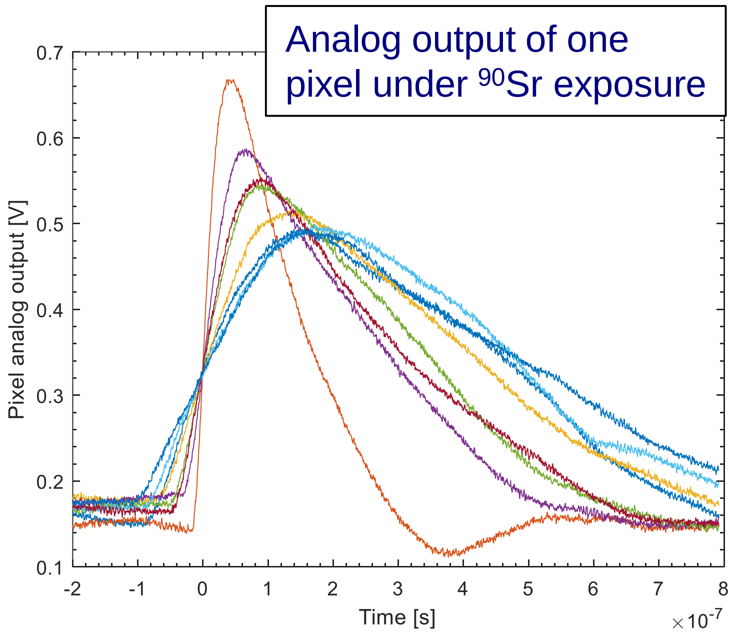
Hit map of the TaichuPix-2 under X-ray from the X-tube voltage of 8 kV for 5 min.

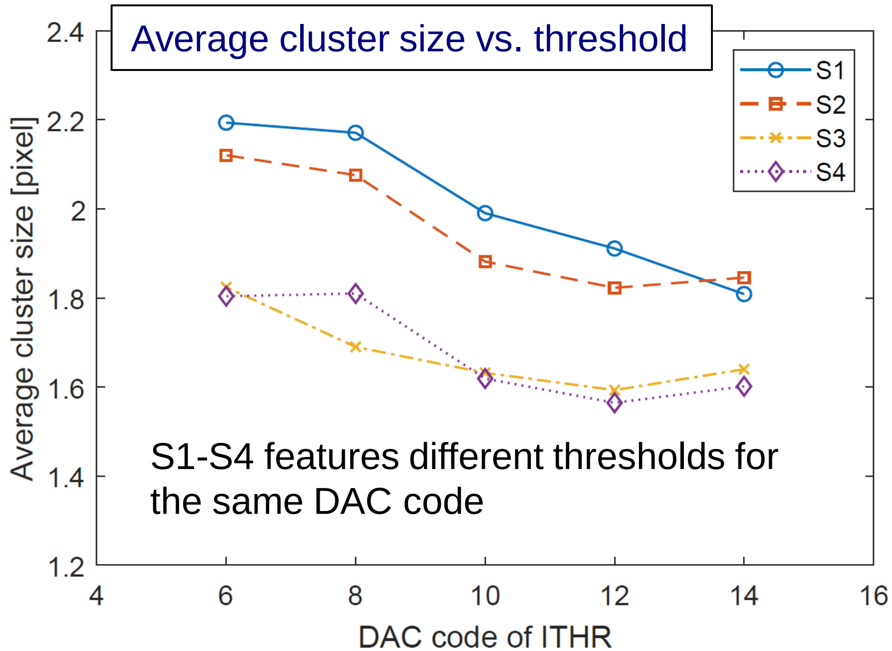


Letter imaging obtained with a 1064 nm laser spot scanning on the TaichuPix-2

TaichuPix2 test with ^{90}Sr

- **TC2 exposure to ^{90}Sr source at different threshold setting (ITHR)**

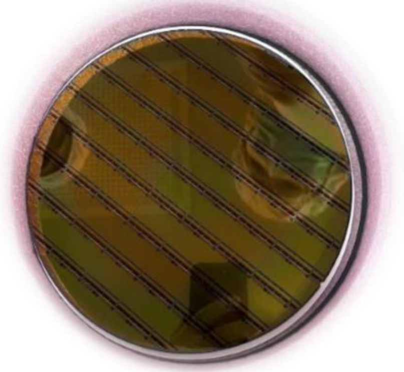




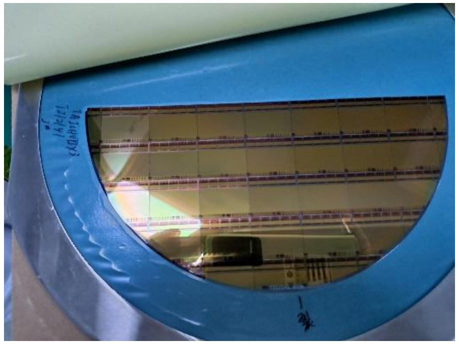
- Shape and amplitude of analog signal as expected, but peaking time and pulse length larger than simulation.
- Average cluster size decreases with threshold as expected
- **Average cluster size for S1-S4 less than 3 as expected**
  - **Indicates the estimated maximum hit rate (36 MHz/cm^2) reasonable**
  - **Cluster size >1, benefits the spatial resolution (better than $pitch/\sqrt{12}$ = 7.2 μm)**

Large-scale sensor TaichuPix-3

- **6 TaichuPix-3 wafers arrived at IHEP in July**
  - **One wafer thinned down to 150 μm and diced**



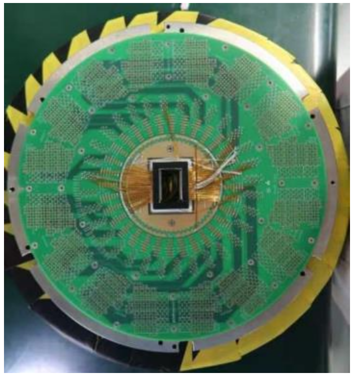
8-inch wafer



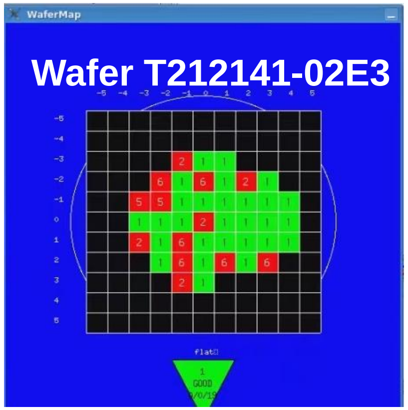
Wafer after thinning and dicing

Thickness after thinning

  - **Complete wafer testing on probe-station →** chip selecting & yield evaluation



Probe card for wafer test



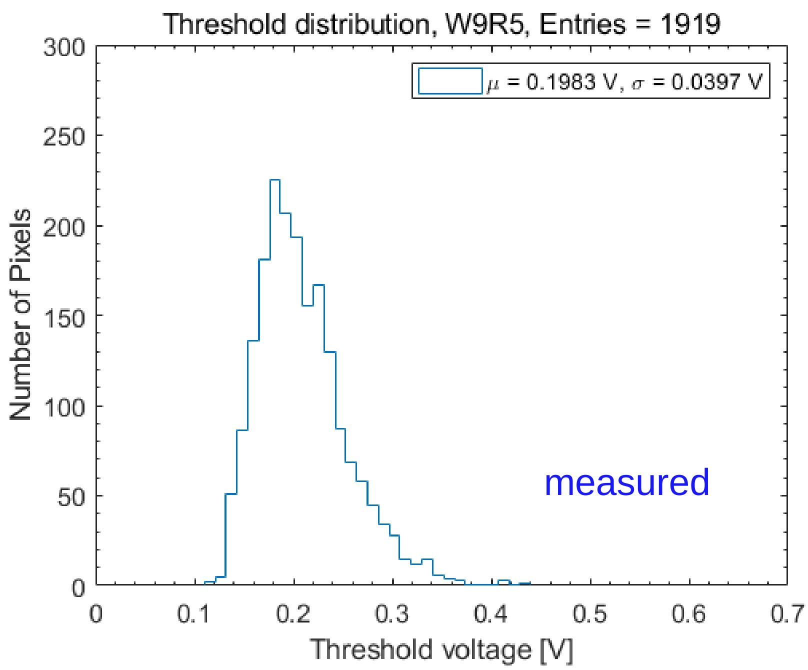
An example of wafer test result

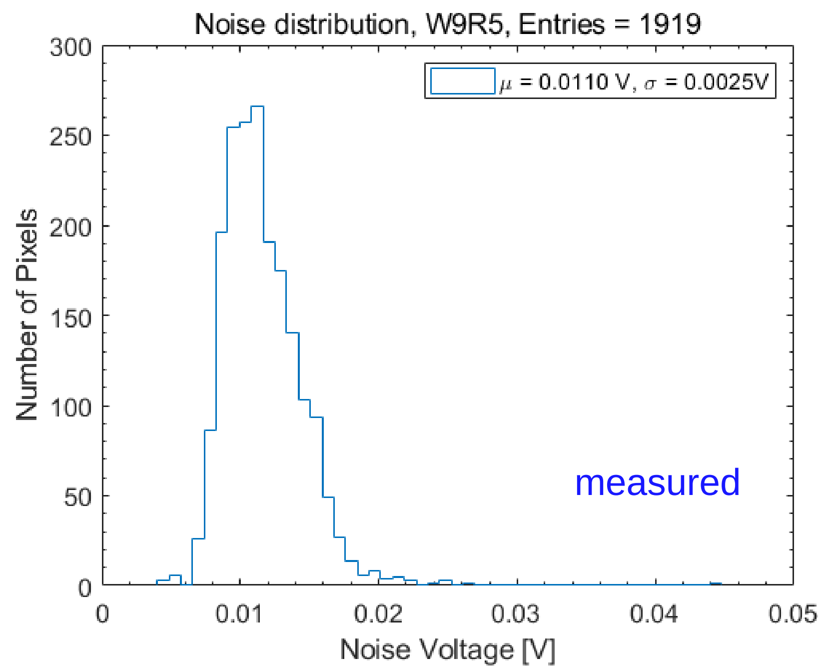
5 wafers tested

- 2 wafer based on standard process
  - Reasonable yield achieved
- 3 wafer based on modified process
  - Preliminary result indicates lower yield than the std. process

TaichuPix-3芯片像素阈值和噪声

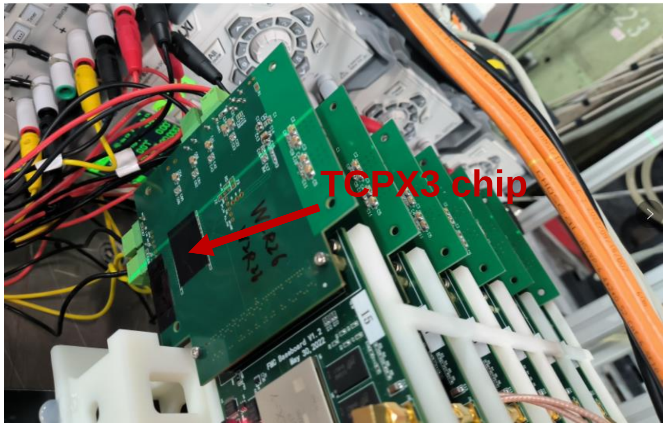
- **Pixel threshold and noise were measured with selected pixels**
  - Average threshold ~215 e$^-$, threshold dispersion ~43 e$^-$, temporal noise ~12 e$^-$ @ nominal bias setting





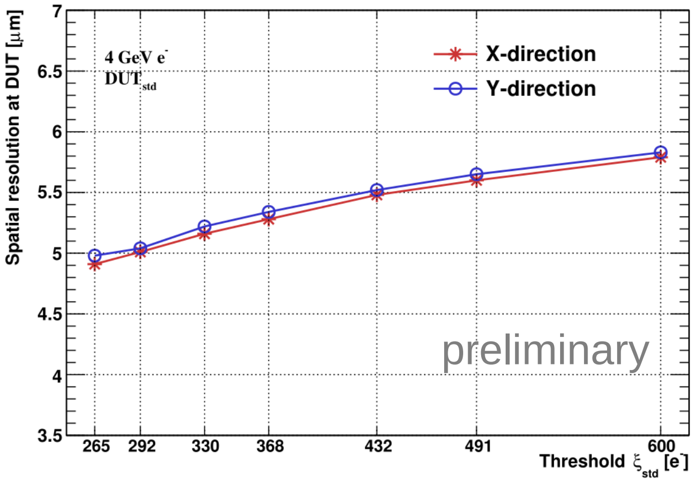
TaichuPix-3 telescope

- The 6-layer of TaichuPix-3 telescope built
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

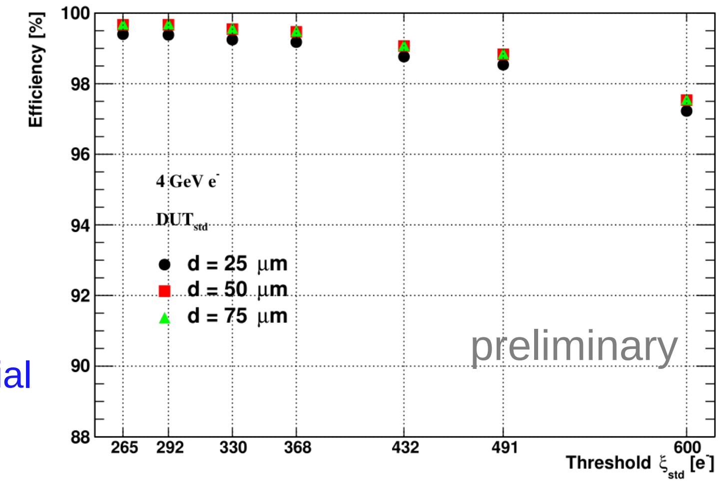


6-layer TaichuPix-3 telescope

- TaichuPix-3 telescope achieved the expected goal in the DESY testbeam
  - Basically works well during the beam test time
  - The preliminary offline results indicate the best spatial resolution could be < 5 μm



Spatial resolution vs. pixel threshold

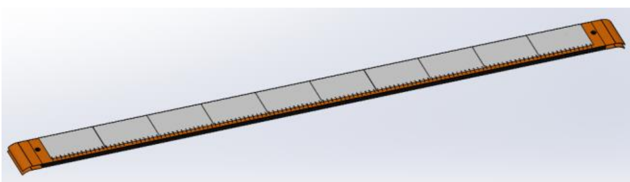


Detection efficiency vs. pixel threshold

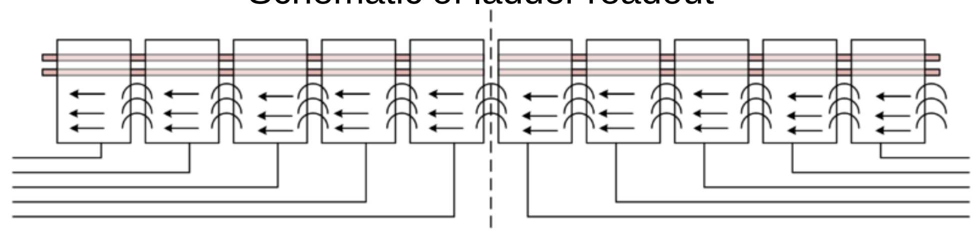
Ladder readout

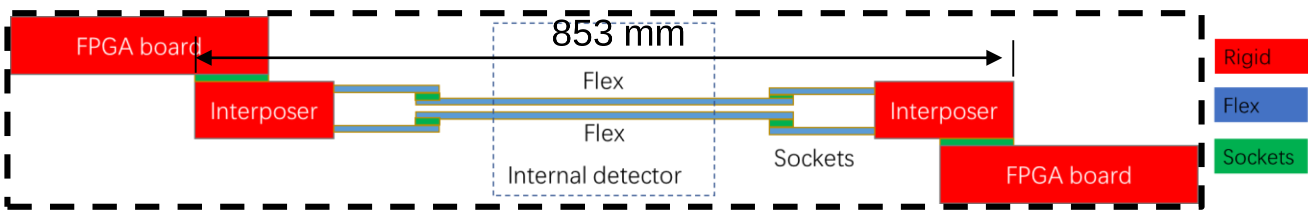
- **Completed detector module (ladder) design**
  - Detector module (ladder) = 10 sensors + readout board + support structure + control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB

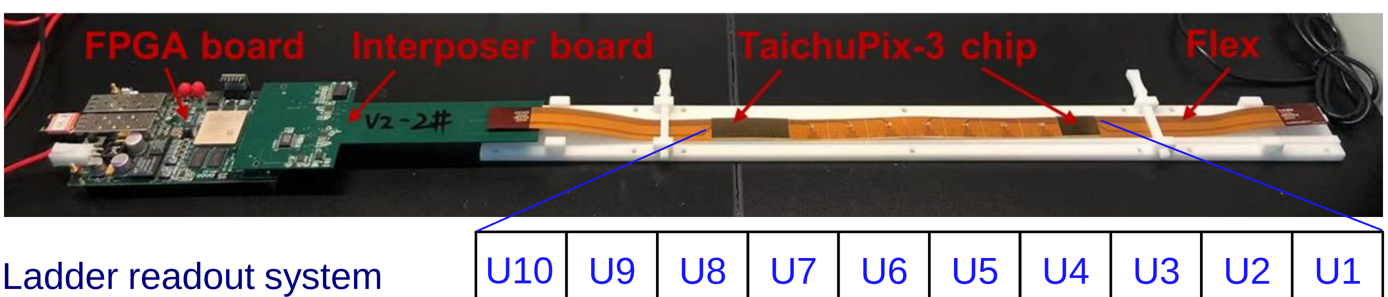
3D module of the ladder



Schematic of ladder readout



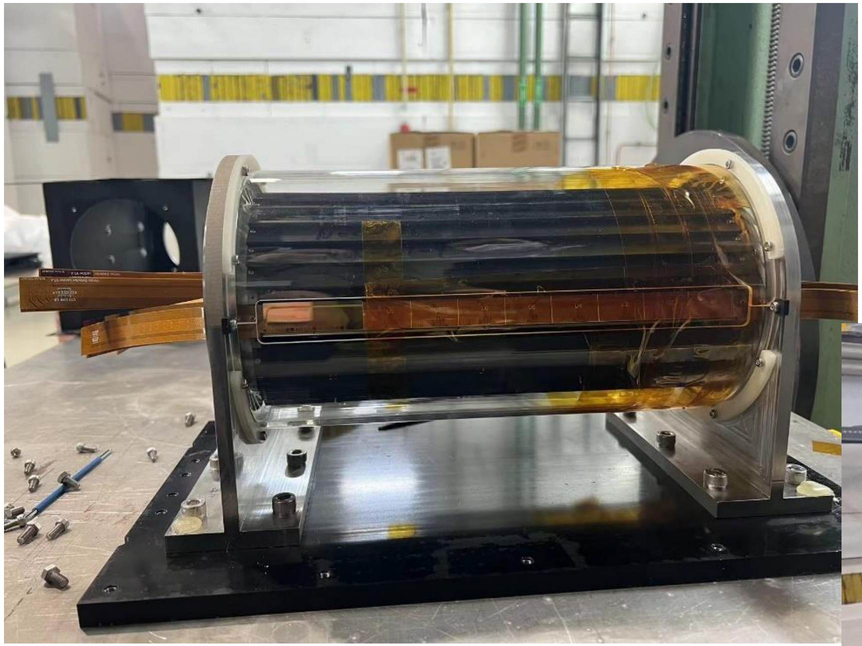




Ladder readout system

Detector prototype

- **6 double-sided layers assembled on the detector prototype**
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector



总结与展望

- **面向CEPC顶点探测器需求，基于MOST2项目支持，开展TaichuPix芯片研发**
  - 采用单片式 CMOS像素探测器技术
  - 像素尺寸 25 µm × 25 µm, 读出时间 50 ns/pixel
  - 经过三次流片实现了全功能全尺寸（25.7 mm × 15.9 mm）芯片，满足设计指标
- **基于全尺寸太初芯片初步研制了束流望远镜和探测器原型样机**
  - 2022年12月对束流望远镜进行了电子束流测试
  - 2023年4月对探测器原型样机进行了电子束流测试

详细内容→ 5月13日下午吴天涯报告

- **展望**
  - 进一步完成完整版探测器模块的研制和原型样机安装
  - 优化Ladder读出
  - 提高探测器系统稳定性